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A MULTIFUNCTION, VME-BASED I/O CONTROLLER WITH 32 PROGRAMMABLE CHANNELS OF ANALOG TO DIGITAL CONVERSION FOR AN UNMANNED AERIAL VEHICLE

THESIS FOR MASTER OF SCIENCE DEGREE

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Faster, more powerful processors are being incorporated into embedded computer systems to execute increasingly complicated algorithms in real time, resulting in a need to transfer more data between the embedded computer and external sensors and servos at a faster rate. To meet these real time requirements, while decreasing the size of the embedded computer hardware, a multifunction, VME-based I/O controller and A/D conversion system was designed, developed, and tested which controls 16 channels of pulse width modulated output, 32 single-ended input channels of A/D conversion with programmable gain and offset capability, and 8 discrete output channels on a single, 6U Versa Module (VME) card. The system is controlled by the Motorola MC68332 32-bit mircocontroller and performs 32 channels of A/D conversion at a 240 Hz rate and 16 channels of PWM at a better than 50 Hz rate. This I/O system was specifically designed to be integrated into the flight control computer of an unmanned research vehicle and pushes state-of-the-air in functionality for real-time, embedded VME-based I/O systems.

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ABSTRACT

Robertson, Melanie M. M.S.C.E., Department of Computer Science and Engineering, Wright State University, 1992. A Multifunction, VME-based I/O Controller with 32 Programmable Channels of Analog to Digital Conversion for an Unmanned Aerial Vehicle.

Faster, more powerful processors are being incorporated into embedded computer systems to execute increasingly complicated algorithms in real time, resulting in a need to transfer more data between the embedded computer and external sensors and servos at a faster rate. In the past, this I/O bottleneck problem has been solved by distributing the I/O tasks among several peripheral controllers to maintain real time operation without burdening the main processor. This type of solution meets the real time requirement, but significantly increases the size of the embedded computer hardware. One of the goals of this thesis was to research, design, and develop an I/O controller that meets the real time requirements of an existing embedded computer system on an unmanned aerial vehicle (UAV), while significantly reducing the size of the associated hardware. The second goal was to incorporate programmability into the gain and offset on the analog to digital (A/D) conversion module of the controller to eliminate time-consuming, manual calibrations and to allow for modification or addition of analog inputs without having to change the hardware. A final goal was to enhance the current pulse width modulation (PWM) and A/D conversion capabilities of the flight computer.

For this thesis, a multifunction, VME-based I/O controller and A/D conversion system was designed, developed, and tested which controls 16 channels of pulse width modulated output, 32 single-ended input channels of A/D conversion with programmable gain and offset capability, and 8 discrete output channels on a single, 6U Versa Module (VME) card. The system is controlled by the Motorola MC68332 32-bit microcontroller and performs 32 channels of A/D conversion at a 240 Hz rate and 16 channels of PWM at a better than 50 Hz rate. This I/O system was specifically designed to be integrated into the flight control computer of an unmanned research vehicle and pushes state-of-the-art in functionality for real-time, embedded VME-based I/O systems.

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1.0 INTRODUCTION

1.1 BACKGROUND

The Flight Dynamics Directorate (FIGL) of Wright Laboratory at Wright Patterson Air Force Base, utilizes the Unmanned Research Vehicle (URV) shown in Figure 1 to conduct experiments in flight control and aerospace vehicle management. By using an unmanned aerial vehicle, new control algorithms and sensor technology can be tested with minimal risk, lower costs, and less time than manned flight tests.

URVs must be light in weight in order to keep airframe and engine construction costs down. However, as new algorithms and functions are added to the URV, the volume of microelectronics onboard also increases. Newer and smaller technologies must be incorporated in order to maintain or shrink the amount of space used by onboard computers. This problem is especially true with I/O, since the amount of external data that the new flight control algorithms must use has gradually increased.

The URV at Wright Laboratory's Flight Dynamics Directorate has an onboard VME-based multiprocessor flight control system (MCS). A top-level diagram of this system is given in Figure 2. The hardware that controls the I/O between the flight control computer (FCC) and the aircraft occupies two and a half slots of an 8-slot VME chassis. The maximum height for each slot is 6U (9.2" x 6.3"). Once slot can be filled

by two half-height, 3U-size cards (3.9" x 6.3").

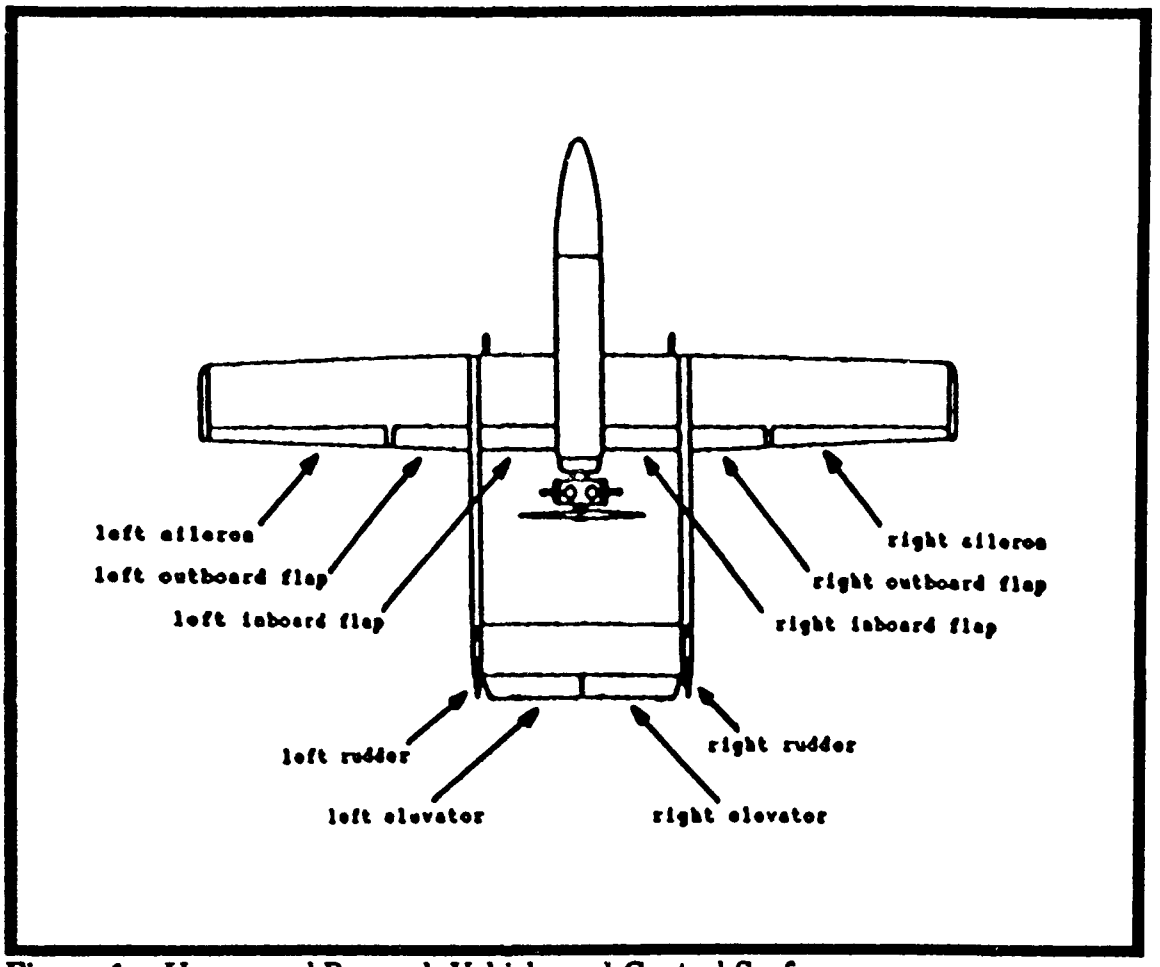


Figure 1. Unmanned Research Vehicle and Control Surfaces

The top half of the first slot is occupied by CPU1, which contains a Motorola 68000 microprocessor and acts as the bus master, controlling all the traffic on the bus. The bottom half of this slot contains the pulse width modulation card which generates 13 channels of pulse width modulated signals and sends them to the servos on the aircraft to change the deflection of 13 control surfaces, ten of which are shown in Figure 1. The three additional control surfaces not shown are the throttle, brake, and steering. The third slot is occupied by CPU3, which also contains a Motorola 68000

microprocessor and transmits and receives telemetry to and from the ground station.

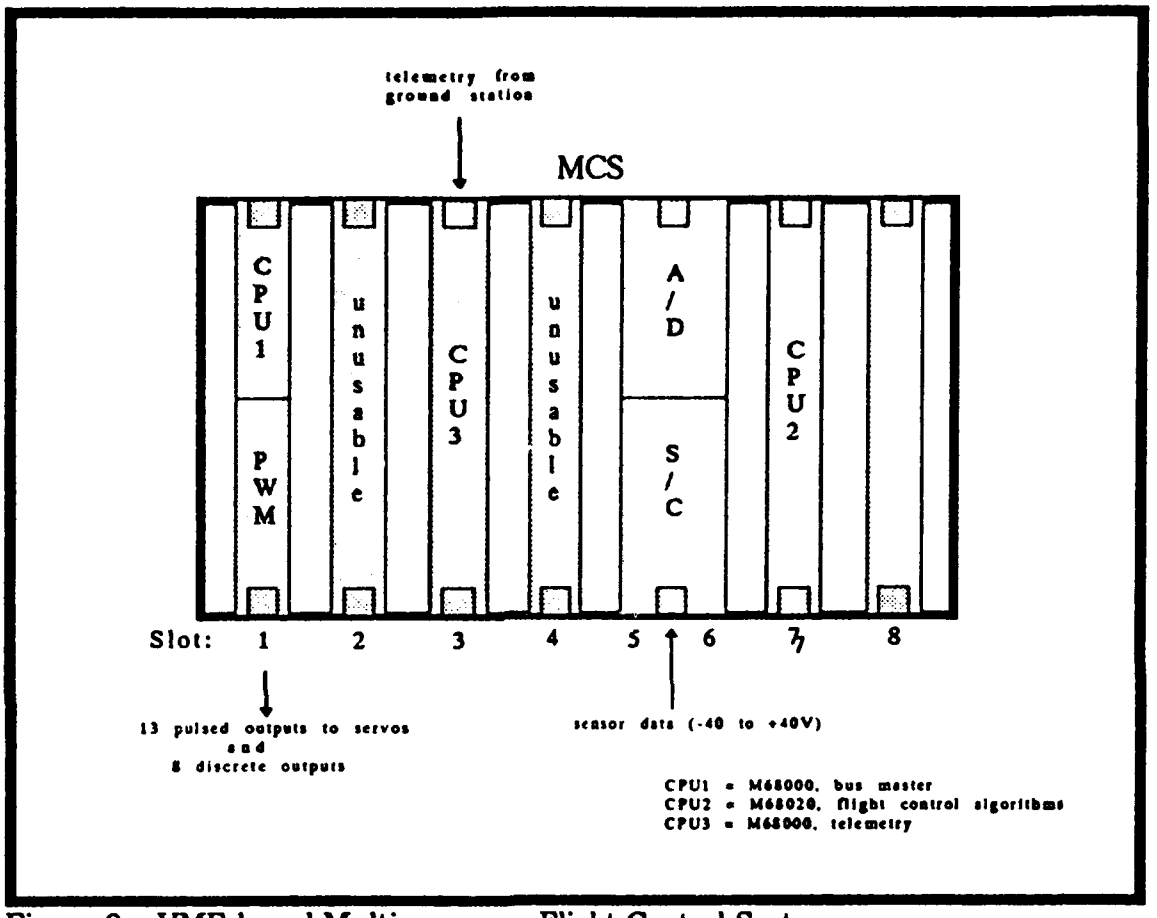


Figure 2. VME-based Multiprocessor Flight Control System

Because the CPU3 card contains wire wrap pins on the bottom and a connector on the top, it extends into the second and fourth slots, making them unusable. The top half of the fifth and sixth slot contains an A/D conversion card which converts 32 channels of analog signals to 12-bit digital words. The bottom half of the fifth and sixth slot is for signal conditioning, which is done on each of the 32 signals before they are fed into the A/D converter. The signal conditioning consists of 32 voltage dividers, low pass filters, and gain and offset potentiometers. Each channel has its own discrete

signal conditioning circuitry. The seventh slot contains CPU2, which is a Motorola 68020-based card, and performs all of the flight control algorithm calculations. Slot 8 is currently unused.

Slots 2-8 on the MCS contain slave cards which must be polled by a separate CPU master to access their data. CPU1 in slot 1 is the bus master and it synchronizes and controls task execution and data transfers. CPU1 obtains the telemetry data sent from a ground station through CPU3 and sends the data to CPU2, which calculates new pulse widths to drive the actuators on the vehicle. CPU1 gets these new pulse widths and delivers them to the pulse width modulation (PWM) card. The PWM card generates the pulse width modulated signals and sends them to the servos on the aircraft. Concurrently, the A/D card receives 27 channels of single-ended analog inputs which describe the current state of each servo and provide new sensor and vehicle data. A list of this data is shown in Figure 3. The digitally converted information is retrieved by CPU1 and delivered to CPU2, which verifies that the servos are operating correctly and uses the data in the flight control algorithm calculations.

Due to the size constraints imposed by the URV, the expansion capabilities of the flight control computer are very limited. Currently, only one slot is available for additional hardware. This limited expansion impacts the vehicle's capabilities for testing new flight control algorithms and computer architectures. In order to have a flexible system which can host additional processors, interfaces, or memory, some slots must be freed up. In addition, the current A/D conversion card is extremely limited because each of the 27 channels are hard-wired and therefore cannot be changed

Right Flap 1
Left Flap 1
Right Flap 2
Left Flap 2
Right Aileron
Left Aileron
Right Elevator
Left Elevator
Right Rudder
Left Rudder
Uplink Signal Strength
Alpha
Beta
Alt. Offset
Mag. Field Strength - X
Mag. Field Strength - Y
Mag. Field Strength - Z
RPM
Battery Volts
Alternator Volts
Roll Attitude
Pitch Attitude
Roll Rate
Pitch Rate
Yaw Rate
Airspeed
Altitude

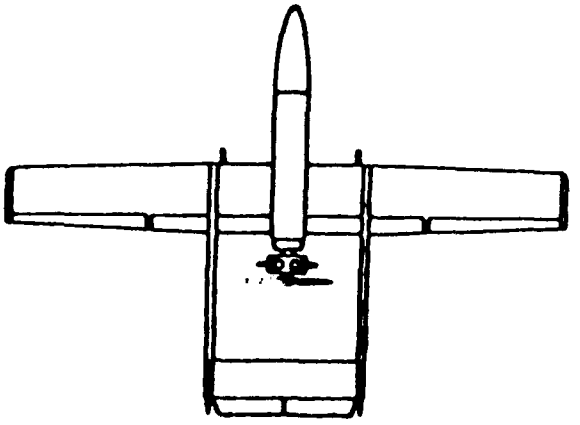


Figure 3. A/D Input Channel Data from the URV

without modifying the hardware. Also, each A/D channel contains potentiometers for gain and offset that must be manually recalibrated before each flight test. This manual calibration is very time consuming and needs to be eliminated. Thus, the need to upgrade and minimize the I/O between the FCC and the URV was identified.

1.2 PROBLEM AND SCOPE

1.2.1 STATEMENT OF PROBLEM

For this thesis, a single, consolidated I/O 6U controller card (9. 3") will be researched, designed, and developed to replace and enhance all of the existing I/O functions on an unmanned research vehicle (URV) flight control computer (FCC). The four functions which will be implemented are signal conditioning, analog to digital (A/D) conversion, pulse width modulation (PWM), and discrete outputs. The first function, signal conditioning, will be conducted on 32 single-ended analog input signals in the -40 to +40 volt range to reduce high frequency noise and to divide the signals down to a usable range by the A/D conversion unit. The second function, A/D conversion, must provide a real-time programmable gain and offset capability and convert 32 channels with a 12-bit resolution and 50 Hz minimum update rate. The third function will provide 16 channels of pulse-width modulated output at a 50 Hz minimum update rate. Finally, the fourth function will provide 8 discrete outputs. In addition, the I/O controller will make data available for offboard processors to access through the VME bus, will be able to receive real time updates for the PWM, gains, and offsets from offboard processors, and will be designed with a control unit to control board level operations.

1.2.2 SCOPE

The I/O controller system designed and developed for this thesis was wire-

wrapped on a perforated board. Although it could be flight tested if the connections were firmly glued in place, the purpose was not to develop a flyable version but to prove that the design and implementation works within the desired specifications. FIGL has plans to have the board manufactured for future use in their existing FCC. The prototype board can, however, be used in the laboratory for development and testing of FCCs.

This I/O controller card was designed under three major constraints. First, the system needed to fit on a single 6U VME card in order to take up less space than the existing I/O functions. Second, the pulse width modulation and A/D conversion functions had to meet a 50 Hz update rate timing constraint. Since the flight control computer executes the flight control algorithms once every 20ms, the I/O to and from the FCC must be sent and received at a 50 Hz rate or better to guarantee that new PWM signal data is sent to the actuators and that new sensor data is being calculated every 20ms. Third, the I/O controller card had to operate within the existing VME-based FCC architecture which treats the I/O as a slave device and polls devices when information is needed.

1.3 GENERAL APPROACH

A market survey in October of 1991 revealed that there is no commercial equivalent to this I/O controller board. In fact, no commercial I/O controller boards could perform 16 channels of pulse width modulation. The main reason for this deficiency is that prior to 1992 when the MC68332 microcontroller was released, no microcontroller had the capability to do 16 channels of pulse width modulation. Even

today, the MC68332 is still the only microcontroller with this capability. Also, there are no known VMEbus boards or off-the-shelf boards available commercially based on the Motorola MC68332. Since Motorola also designed the MC68332 with the capability to provide stepper motor control and angle-based engine control, it is expected that this microcontroller will be used by the automotive industry in future automobiles.

In the beginning of 1992, the MC68332 chip was only available in a surface mount package, and the carriers to convert from surface mount to through-hole were very expensive. So instead of using the MC68332 chip, a development board containing a business card computer (BCC) based on the MC68332 was obtained because it was more cost effective. The BCC is a stand-alone computer named for its business card dimensions and contains the MC68332, 32k x 16 of ROM, 64k x 16 of RAM, and a monitor called 332Bug. A diagram of the BCC is shown in Figure 4. The advantage to using the BCC over just the MC68332 chip is the capability to use its monitor debug tool for system development. There are some disadvantages, however, because the BCC does not allow the designer to use the full capabilities of the MC68332. These disadvantages will be elaborated on in Section 3.

All of the components for the I/O controller were researched and purchased in early 1992. The design of the system was performed on a schematic CAD tool called FutureNet to facilitate building and testing of the board. FutureNet provides the capability to draw the design and provides a pin-to-pin connection list for building and testing of the design. The signal conditioning and A/D conversion units of the I/O controller system were breadboarded to prove that the design worked and to get test results before the board was ever built. A board layout was designed that placed all

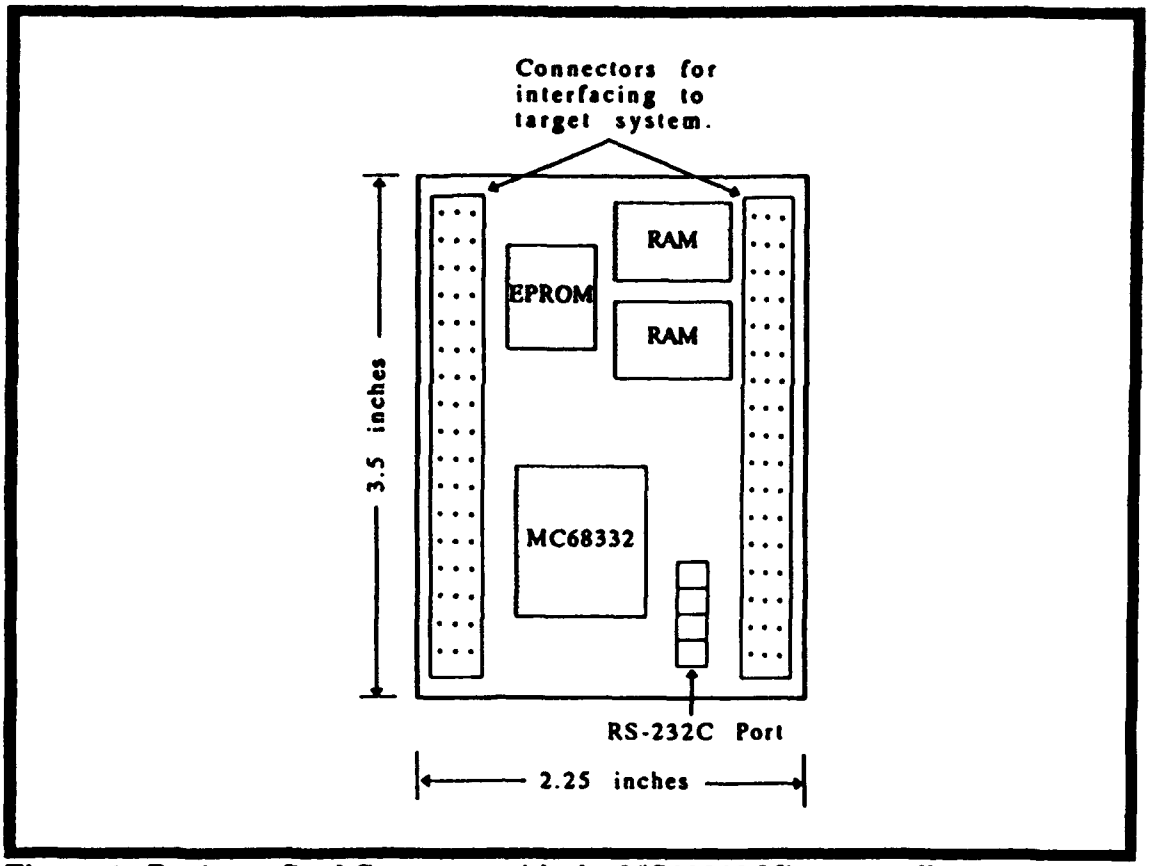


Figure 4. Business Card Computer with the MC68332 Microcontroller

42 of the chips used at the best location on the board. After the board was wirewrapped, the hardware was debugged and tested in a VME rack and interfaced to by a MC68030 board. The embedded software to control the A/D conversion and PWM was written in MC68332 assembly language.

1.4 SEQUENCE OF PRESENTATION

Section 2 of this thesis contains a more detailed discussion of the conditions under which the I/O controller system will be used and the exact design requirements. In Section 3, the hardware design is explained and performance results are provided.

Section 4 provides the software design at the flowchart level. Section 5 summarizes the main features of the I/O controller and its performance and provides conclusions and recommendations for further research and modifications. Appendix A contains CAD drawings of the hardware schematics. Appendix B contains a list of all the parts used in the I/O controller. Appendix C contains a bibliography of the literature researched to survey the market. Appendix D contains the printed circuit board layout showing the location of chips on the board. Throughout the text, the asterisk '*' denotes low active signals and the dollar sign '$' precedes HEX numbers.

2.0 DESIGN

Current VME-based IO systems on the market are limited in that they usually only provide one capability, such as A/D conversion or serial I/O. No system is available on a single 6U VME card which combines 16 channels of pulse width modulation (PWM) and 32 channels of A/D conversion. Thus, it was necessary to design and develop such an I/O system to upgrade the current flight control computer (FCC) I/O capabilities.

An FCC I/O controller which meets the requirements specified in the statement of problem could be partly designed on an ASIC chip to save board space. For research and development though, the ASIC alternative is too expensive and cannot be considered. Therefore, the design had to be completed with commercially available off-the-shelf (OTS) parts. Since this version is a prototype it does not have to be flight qualified and therefore it can be a wire-wrapped board.

The URV I/O controller design must satisfy several requirements as illustrated by the diagram in Figure 5. An interface is necessary to provide access to the VMEbus. This interface must buffer the VMEbus signals and handle the control logic according to the VMEbus Specification ANSI/IEEE Standard 1014 [c]. The I/O controller board must generate 8 discrete outputs and 13 channels of Pulse Width Modulation (PWM). The controller must be able to perform 32 channels of A/D conversion and provide programmable gain and offset. Finally, the inputs and outputs

on the I/O controller must be handled once every 20 ms to satisfy the update

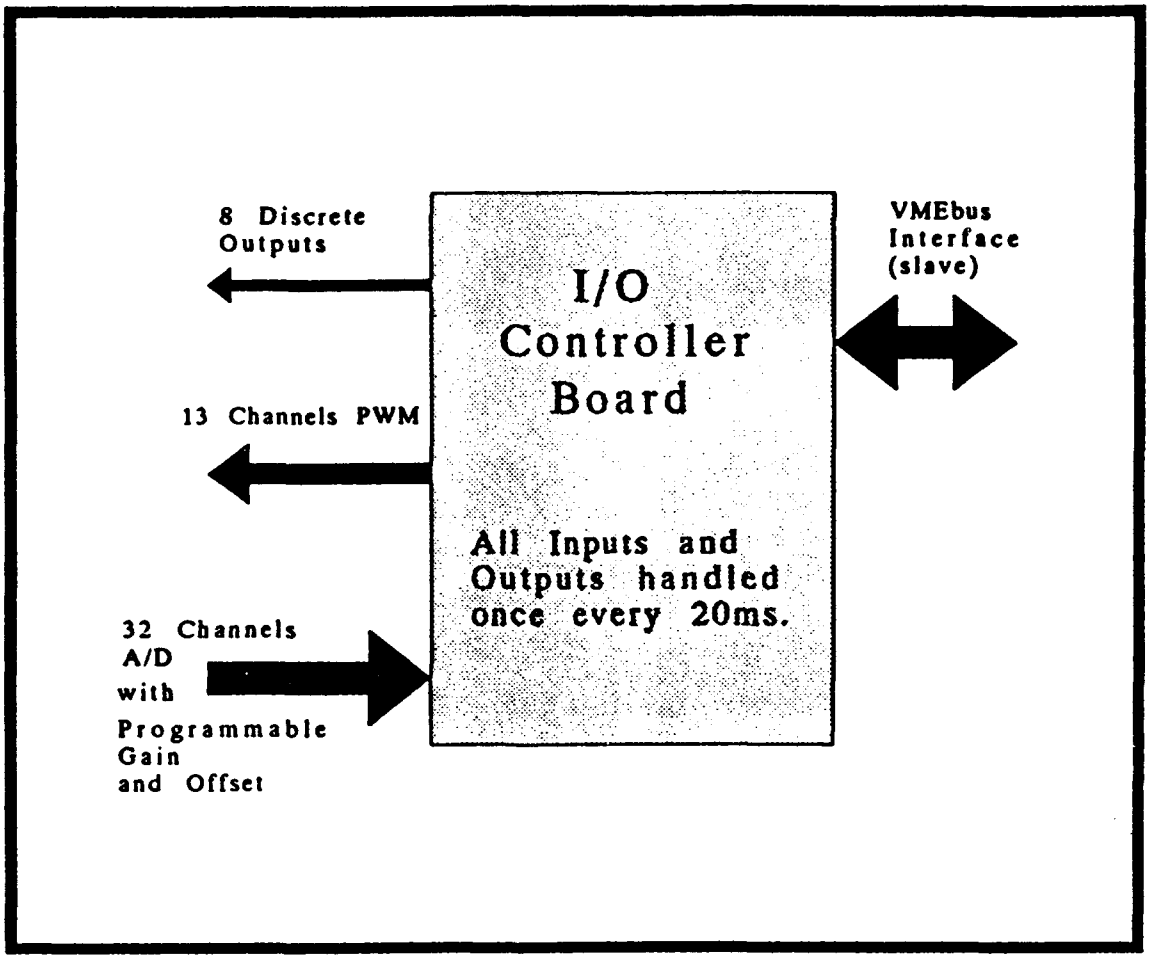


Figure 5. Design Requirements

requirement of the flight control computer.

Figure 6 provides a top level design of the I/O controller that meets the functional requirements. An onboard control unit is necessary to generate 8 discrete outputs and control the pulse width modulation (PWM) Unit and the A/D Conversion Unit. Transfer of information to and from the I/O controller is done via a shared memory that can be accessed by offboard processors across the VMEbus and the onboard Control Unit. The VMEbus Interface Unit is responsible for address decoding

such data transfers and storing the data in shared memory. Input data for the PWM unit is sent once every 20ms from the M68000 offboard processor (CPU1 - bus master) across the VMEbus to the I/O controller. The initiator of this data transfer must be the offboard bus master, since the I/O controller is a slave card and cannot fetch the PWM data from the master.

Similarly, output data from the A/D Conversion Unit must be fetched periodically by the bus master. Again, the I/O controller cannot send this data, so the data must be available to the VMEbus Interface Unit upon a request from the main CPU. Therefore, the Control Unit must update the shared memory with all 32 A/D conversions at a better than 50 Hz rate so that new data will be available when the main CPU fetches it every 20ms. The embedded software for the control unit is stored on EPROM.

The Signal Conditioning (S/C) Unit is comprised of discrete, passive devices which are necessary to filter out high frequency noise and to divide the analog input signals down to levels that can be used by the integrated circuits (ICs) in the A/D Conversion Unit.

Several devices were researched to determine what parts were available to meet the functional and physical design requirements. The final parts list can be found in Appendix C. The choice for the control unit was very limited because the Motorola MC68332 microcontroller is the only controller capable of performing 16 channels of PWM. Trying to design the PWM unit separate from the controller takes up too much board space.

To save additional board space, the MVME6000 VMEbus interface device was chosen because it performs all of the necessary logic to interface with the VMEbus in

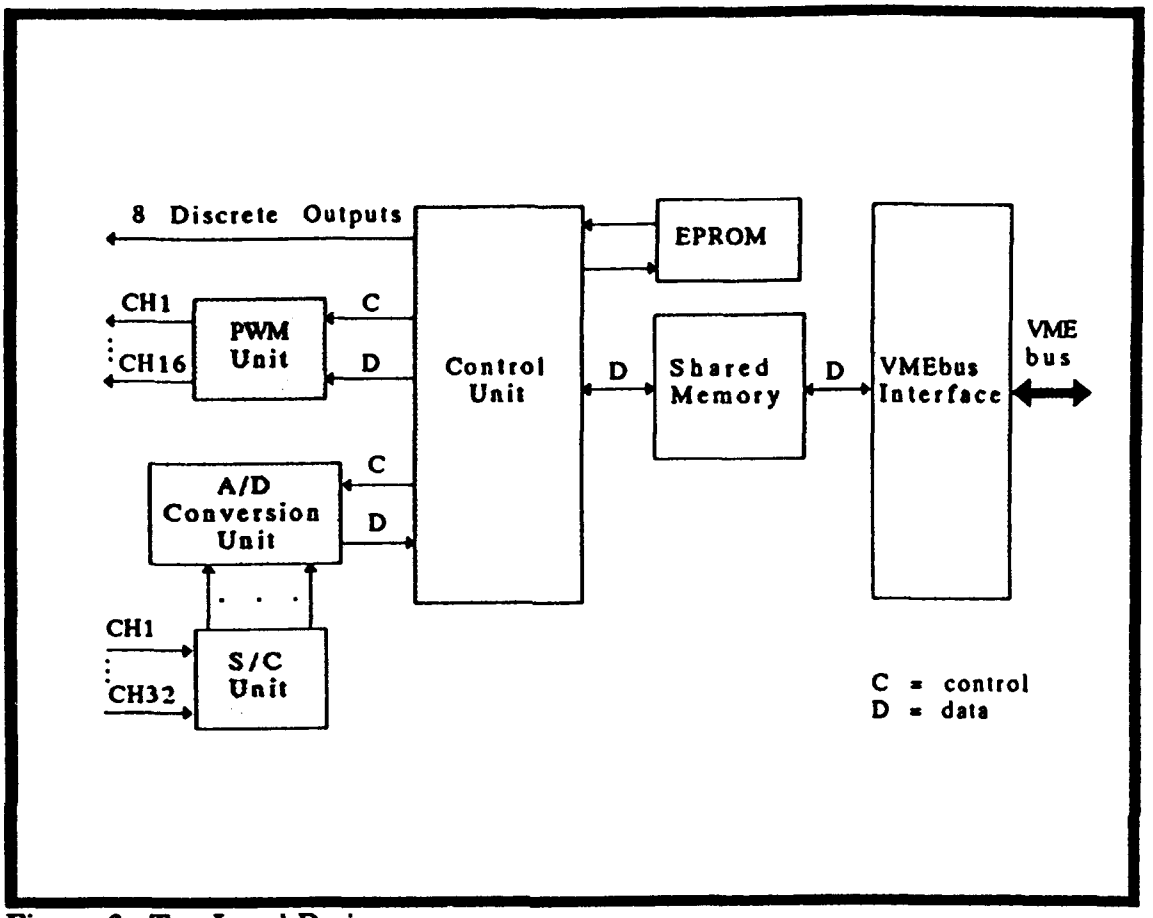


Figure 6. Top Level Design

one chip. The alternative is to use discrete logic or programmable logic devices, but each would take up too much board space.

A Dual Port RAM (DPRAM) can be used as the shared memory to provide access to memory without memory conflicts because the DPRAM locks access to an address that is already in use. The MC68332 will connect to one side of the DPRAM and the MVME6000 to the other. An onboard EPROM is necessary to store the executable code for the MC68332 to access on power-up. In order for the board to be flight tested, it must have the capability to boot and initialize itself and start execution of the embedded control software stored in the EPROM.

A multiplying digital to analog converter (DAC) was chosen to perform the programmable gain amplification because it is suitable for reference input signals that fluctuate and can interface directly with a microprocessor. The DAC chosen has a 12-bit resolution. Providing the analog input with a gain before the A/D conversion takes place is necessary to take advantage of the full 12-bit A/D conversion resolution. A fixed reference DAC is needed for the programmable offset (PO) to generate an offset voltage for different digital inputs and a fixed-reference analog input. The DAC chosen for the PO also has a 12-bit resolution and the capability to sum its output with another signal. Both of these DACs provide a low-cost means of interfacing between the digital and analog circuitry.

Providing separate circuitry for each channel of A/D conversion takes up far too much board space. Therefore, the analog inputs will be processed serially, one after the other, with the same circuitry. To accomplish this, the signals must be multiplexed from 32 to 1 with MUX devices. As long as all 32 channels can be updated within the minimum update rate, this solution is optimal.

3.0 HARDWARE

3.1 MC68332 MICROCONTROLLER UNIT

The I/O controller design was based on the Motorola MC68332 microcontroller unit (MCU), which is a 32-bit integrated microcontroller that provides high-performance data manipulation capabilities. The MC68332, or MCU, is mostly instruction set compatible with the Motorola M68020 and entirely with the Motorola M68010. The MCU contains four intelligent stand alone subsystems which are ideally suited for this application because they can perform in real time, but in the background so that its central processing unit (CPU32) is able to control multiple tasks. This feature is necessary in order to perform simultaneous input and output with a single microcontroller.

A block diagram of the MC68332, which identifies each subsystem, is shown in Figure 7. The Time Processor Unit (TPU) subsystem controls 16 independent, orthogonal channels, each with a dedicated I/O pin and capable of performing any one of the following time functions: Discrete I/O, Pulse Width Modulation, Input Capture/Input Transition Counter, Period Measurement with Additional Transition Detection, Period Measurement with Missing Transition Detection, Position-Synchronized Pulse Generator, Stepper Motor Control, Output Match, and Period/Pulse Width Accumulator. The TPU will be used to perform the 16 channel

pulse width modulation for the I/O controller.

The MC68332 also includes a Queued Serial Module (QSM) which provides peripheral interface capabilities, a System Integration Module which provides 12 chip selects to reduce the need for external glue logic and an automatic periodic interrupt generation capability, and Standby RAM Module with 2K bytes of fast static RAM.

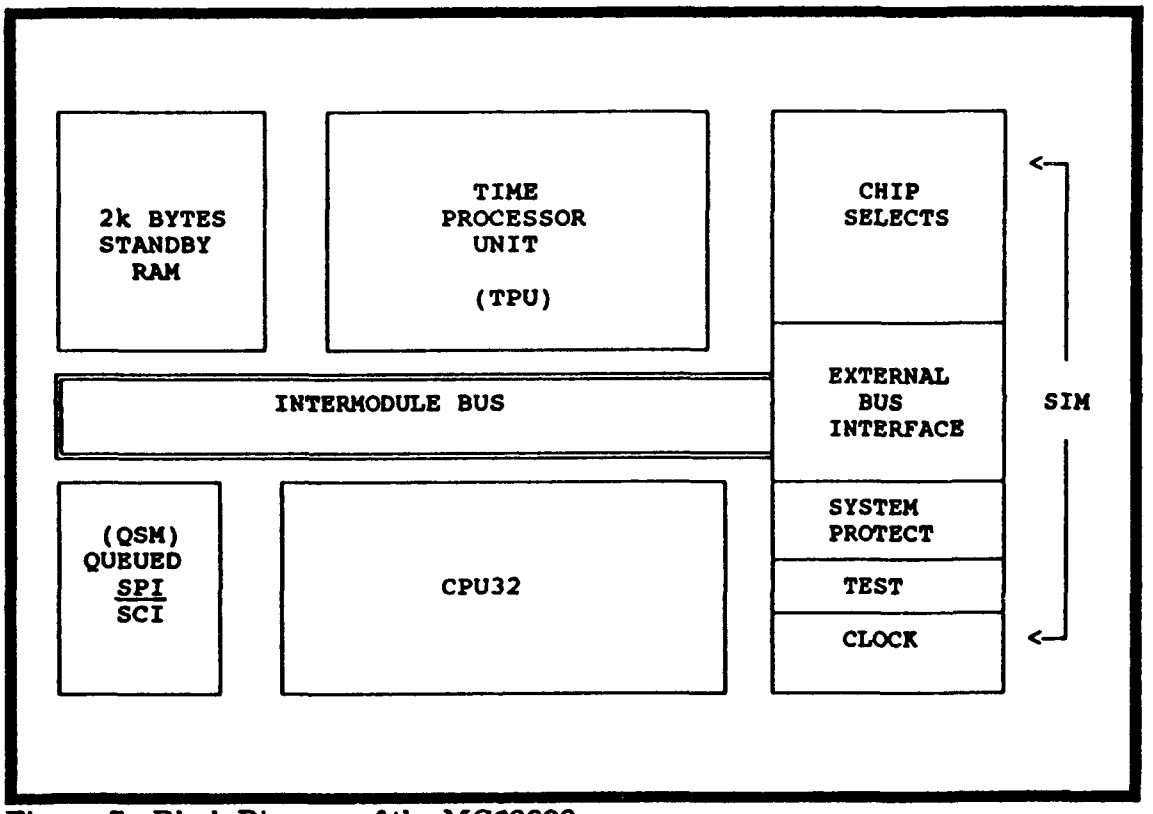


Figure 7. Block Diagram of the MC68332

3.2 BUSINESS CARD COMPUTER

Since the MC86332 has only been on the market for little over a year, there is not much documentation and there are very few applications which use it. In order to speed up development, a business card computer unit containing an MC68332 running at 16.78MHz, a 64Kx16 EPROM, and a 32Kx16 RAM was used in the design and development of the I/O controller in place of a sole MC68332 chip. The most important feature of the BCC is that it contains a monitor called 332DIBUG, which provides excellent debugging capabilities because it is bootable and can be used to read the EPROM and modify RAM on the I/O controller card during testing.

3.3 CHIP SELECTION AND DSACK GENERATION

To generate the chip selects for the I/O controller, the capability of the MC68332 to provide 12 chip selects, 11 user defined and one for booting from a ROM, was utilized. These chip selects also have the capability to automatically generate DSACKX* (data transfer and size acknowledge) after a certain number of wait states, excluding the need to use external logic. DSACK0* and DSACK1* are input pins to the MC68332 that notify the processor that the data has been latched from the data bus by the external device on a write cycle or that the data is ready to be read on a read cycle. After DSACKX* is asserted, it must then be negated within 80ns after AS* and DS* are negated or the MC68332 will issue a bus error (BERR*). The negation of DSACKX* is also handled by the MC68332 chip selects automatically.

The BCC uses CS0* - CS2* (chip select line 0 - chip select line 2) and

CSBOOT*, but the remaining eight chip selects are available. The minimum CS* hold time must be considered for each device in order to determine how many wait states should occur before DSACKX* is asserted. Each wait state is 59.6ns.

To initialize an MC68332 chip select, two registers must be written to in the SIM Unit. These are the Chip Select Base Address Register (CSBAR) and the Chip Select Option Register (CSOR). The CSBAR identifies the address range to be decoded based upon the base address plus a selectable block size. The CSOR sets up the remaining control factors including whether or not the chip select will be generated on read, write, or both read and write, and how long to wait before DSACKX* is generated. Table 1 shows the initialization values of the chip selects used in the I/O controller. The corresponding address ranges defined by the CSBAR value for the chip selects are shown in Table 3.

CSBAR	Address	Value	CSOR	Address	Value
CSBAR3	$FFFA58	$0820	CSOR3	$FFFA5A	$7BF0
CSBAR4	$FFFA5C	$0828	CSOR4	$FFFA5E	$71F0
CSBAR5	$FFFA60	$0830	CSOR5	$FFFA62	$70B0
CSBAR6	$FFFA64	$0838	CSOR6	$FFFA66	$70F0
CSBAR7	$FFFA68	$0840	CSOR7	$FFFA6A	$70F0
CSBAR8	$FFFA6C	$0103	CSOR8	$FFFA6E	$68F0
CSBAR9	$FFFA70	$0801	CSOR9	$FFFA72	$78B0
CSBAR10	$FFFA74	$0848	CSOR10	$FFFA76	$6A70

Table 1. Chip Select Initialization Values

Each of the Chip Select Option Registers (CSORs) are described in more detail in Table 2. A description is provided as to how the CSOR value was chosen based on the minimum CS* hold time for the device being selected and whether it will be read

only, write only, or a read/write device. The appropriate number of DSACKX* wait states (WS) is chosen based on the minimum CS* or WR* hold time (1 DSACKX* WS = 59.6ns). The number of wait states is then used in the CSOR value. The MC68332 will automatically generate DSACKX* after the exact number of wait states have occurred as designated in the CSOR.

Chip Select	Device	R/W Status, Minimum Chip Select Hold Time, and Equivalent Wait States	CSOR Value
CS3*	MVME6000	R/W, External DSACKX* generation	$7BF0
CS4*	PGA	R/W, generate DSACKX* after 400ns = 7 WS (= minimum WR* pulse width)	$71F0
CS5*	PO	Write Only (WO), generate DSACKX* after 100ns = 2 WS (= minimum CS* pulse width)	$70B0
CS6*	MUX1	WO, generate DSACKX* after 400ns = 7 WS (= minimum WR* pulse width)	$70F0
CS7*	MUX2	WO, generate DSACKX* after 400ns = 7 WS (= minimum WR* pulse width)	$70F0
CS8*	EPROM	Read Only (RO), generate DSACKX* after 150ns = 3 WS (= minimum access time)	$68F0
CS9*	DPRAM	R/W, generate DSACKX* after 80ns = 2 WS (= minimum access time including conflict)	$78B0
CS10*	A/D Converter	RO, generate DSACKX* after 520ns = 9 WS (= clocked flip-flop delay + delay through flip-flip (H-L) + maximum RD* to BUSY* propagation delay on A/D = 250ns + 40ns + 230ns)	$6A70

Table 2. Chip Selection Option Registers Note: WS = wait state

3.4 ADDRESS MAP

Table 3 contains the address map for the I/O controller. The 332BUG monitor controls the basic layout of the address space because it initializes the MC68332 chip selects CSBOOT, CS0, CS1, and CS2 to decode its EPROM and RAM after bootup. Some of the address space is invalid because the monitor does not allow access to those addresses. High memory from FFFA00 to FFFFFF is used by the MC68332 to store the registers for its internal modules - SIM, RAM CTRL, QSM, and TPU. Some of this high memory has been reserved by the MC68332. The MC68332 chip selects 3-10 are initialized during runtime of the controller code to select all of the I/O controller selectable devices. The interrupt vector table is located at the beginning of the memory in the target vector table. The vector base register is set to address $0000.

3.5 DPRAM AND EPROM

The dual port RAM (DPRAM) is used because data can be accessed from both sides simultaneously. Connections to the DPRAM are shown in Appendix A, drawing 5. Therefore, the MC68332 will have access to the left side and offboard processors can access the right side of the DPRAM from across the VMEbus through the MVME6000 bus interface device. The same address cannot be accessed by both sides at the same time, but the DPRAM will delay the second request no longer than 80ns. When this happens, DSACKX* will be delayed until the data is either written or placed on the bus for a read. Thus, the hardware efficiently handles memory contentions.

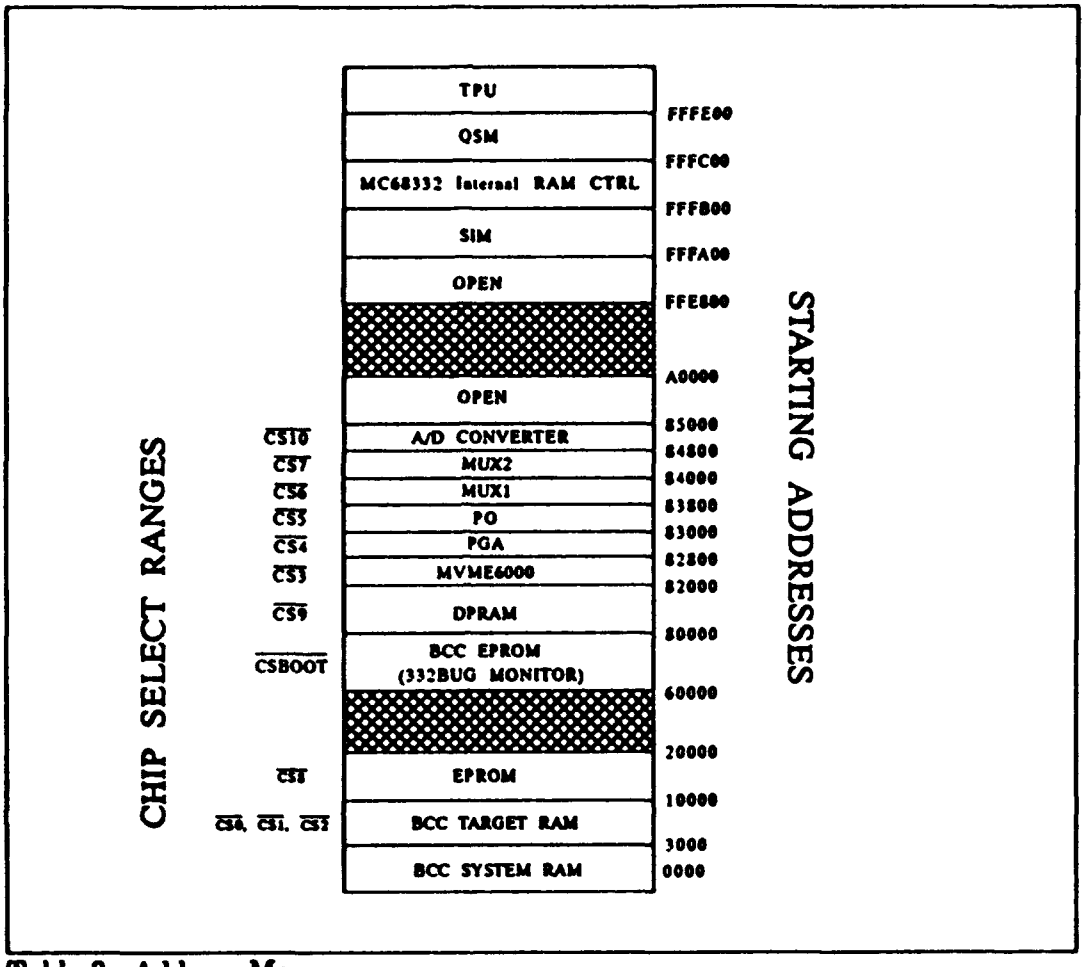


Table 3. Address Map

3.6 PROCESSOR TO VME BUS INTERFACE

The MC68332 must initialize the MVME6000 VMEbus interface because the MVME6000 cannot be accessed by offboard processors until it is initialized. Since this cannot be done through the dual port RAM, a separate access was designed using some buffers to allow one-way communication from the MC68332 to the MVME6000. The buffers are necessary to prevent conflicts on the bus, which would occur if the busses on both sides of the DPRAM were connected. A conflict would occur if the MC68332 tried to access the MVME6000 at the same time that the MVME6000 tried

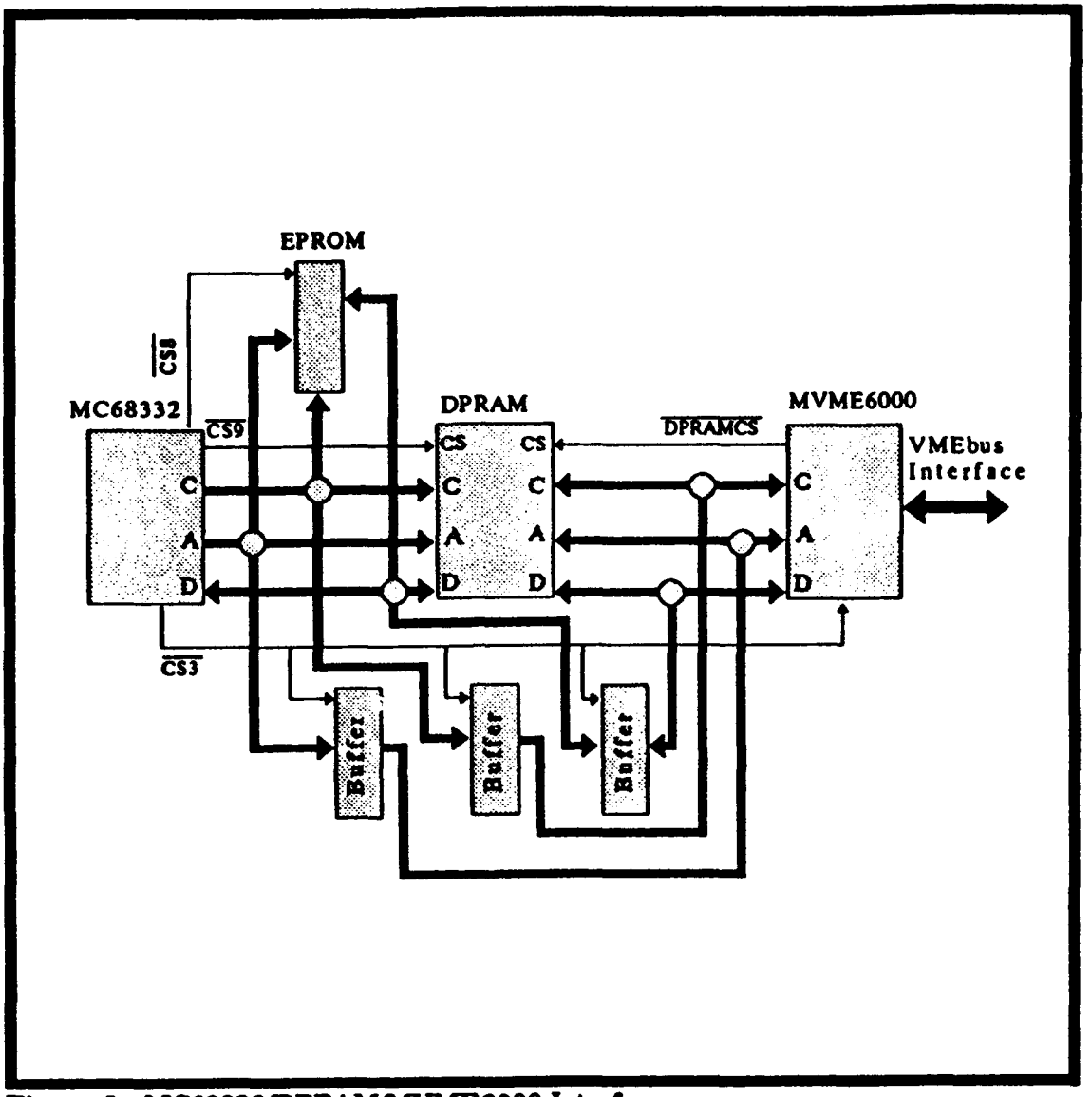


Figure 8. MC68332/DPRAM/MVME6000 Interface

to access DPRAM. Figure 8 shows the interface from the MC68332 to the MVME6000 through the DPRAM and the uni-directional buffers. Appendix A, drawing 5 also contains the schematics for this interface.

3.7 SIGNAL CONDITIONING

Each analog input channel passes through a voltage divider circuit and a low pass filter. The voltage divider divides the 0-±40 volt input signal down to 0-±10 volts, a range that can then be used by the A/D circuitry. Although not all channels have a ±40V maximum input, each channel has been designed to handle such an input so that none of the channels are hardware dependent. According to Kirchhoff's voltage law, when an input voltage is applied across two resistors in series, the resulting current is defined as:

$$i = \frac{v_{in}}{R_1 + R_2}$$

Ohm's law is then used to find the voltage across one of the resistors as follows:

$$v_2 = iR_2 = v_{in} \frac{R_2}{(R_1 + R_2)}$$

(Nilsson, 1986)

To divide the input voltage by four resulting in $v_2 = v_{in}/4$, R1 and R2 must be calculated according to the equivalent resistance desired:

$$R_{eq} = .25\Omega = \frac{R_2}{R_1 + R_2}$$

Solving for R1 yields:

$$R_1 = 3R_2$$

In the I/O Controller hardware, R_1 = 31.6kΩ and R_2 = 10.5kΩ as illustrated in Figure 9, which shows one of the 32 resistor-capacitor (RC) networks from the controller. These values were chosen because they came closest to providing an exact divide by four function in the desired ohm range. One percent metal-film resistors were used to reduce the channel dependent offset differentials. Since the signal conditioning is performed on each channel discretely, it introduces a slightly different offset in each channel. The channel dependent offset differences must be negligible in order for the input signals to be independent of a channel. Using 31.6kΩ for R1 and 10.5kΩ for R2, the nominal channel dependent offset (CDO) in volts is calculated as:

$$CDO = v_{in} \div \left(4 - \frac{10.5 + 31.6}{10.5}\right) = -0.0006v_{in} \text{ [volts]}$$

The CDO is the nominal offset added to each input voltage by the signal conditioning devices. The maximum channel dependent offset differential (CDOD) is calculated using one percent resistances as follows:

$$CDOD_{max} = CDO(R_1+0.01R_1,R_2-0.01R_2) - (R_1-0.01R_1,R_2+0.01R_2) = 0.12v_{in} \text{ [volts]}$$

Based on the result above, it was found that using one percent resistors was not enough to guarantee negligible channel dependent offset differences. Either the resistors in the RC networks must be picked to match better than within one percent tolerance or the offset must be reset in the software when a signal is moved from one channel to another.

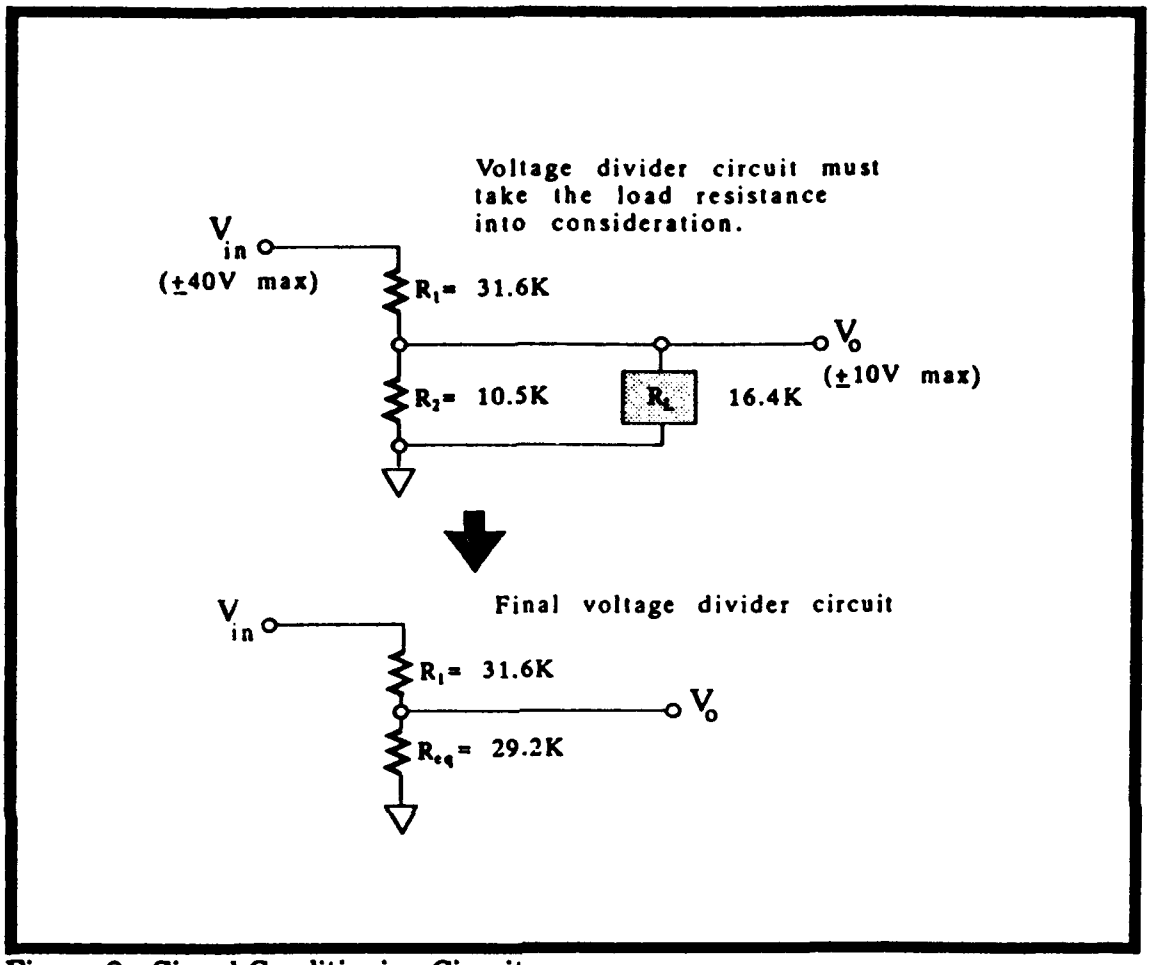


Figure 9. Signal Conditioning Circuit

A low pass filter is necessary to filter out high frequency noise above the frequency range that the input signal is in. Since the analog input signal is at a very low frequency, well below 50Hz, passing a signal below 50 Hz is sufficient. The bypass capacitor necessary to meet this requirement is calculated below using the equation for a low pass filter:

$$f_{cH} = \text{cutoff frequency} = \frac{1}{2\pi R_2 C}$$ [Johnson, 1984]

$$\therefore \quad \text{for } f_{o,H}=50\text{Hz} \quad C = \frac{1}{2\pi(10.5\text{x}10^{3})(50)} = 0.303\mu\text{F} \sim 0.33\mu\text{F}$$

3.8 A/D CONVERSION MODULE

The A/D Conversion module of the I/O controller follows the signal conditioning and converts 32 channels of 0-±10 volt analog signals with 12 bit precision at a better than 50 Hz rate. The A/D Conversion module consists of four stages: multiplexing, programmable gain amplification, programmable offset, and A/D conversion. These stages, their interconnections, and their digital control lines are shown in Figure 10. To conserve space and fulfill the goal of putting the I/O controller on a single 6U VME card, the 32 analog input channels are multiplexed from 32 to 1. This is feasible because each channel can be processed serially and still meet the real time requirement for updating all 32 channels in under 20 ms, while avoiding a parallel architecture which would take up more board space. Since a market survey did not reveal a single multiplexor (MUX) that could handle 40 volt inputs, the signals had to be divided down before multiplexing as described in the previous section. After a signal is switched through the MUX it is amplified by a programmable gain amplifier (PGA) and added to an offset supplied by the programmable offset (PO). The chip select for the A/D converter also commands the sample and hold (S/H) device to hold the signal for conversion. This process occurs periodically at approximately a 240 Hz rate. The MC68332 controls each step by periodically selecting the devices in the proper order and providing adequate delay for each device to process a new signal before digital conversion takes place. The MC68332 has been set to control this process through the use of its Periodic Interrupt Timer in the System Integration Module (SIM).

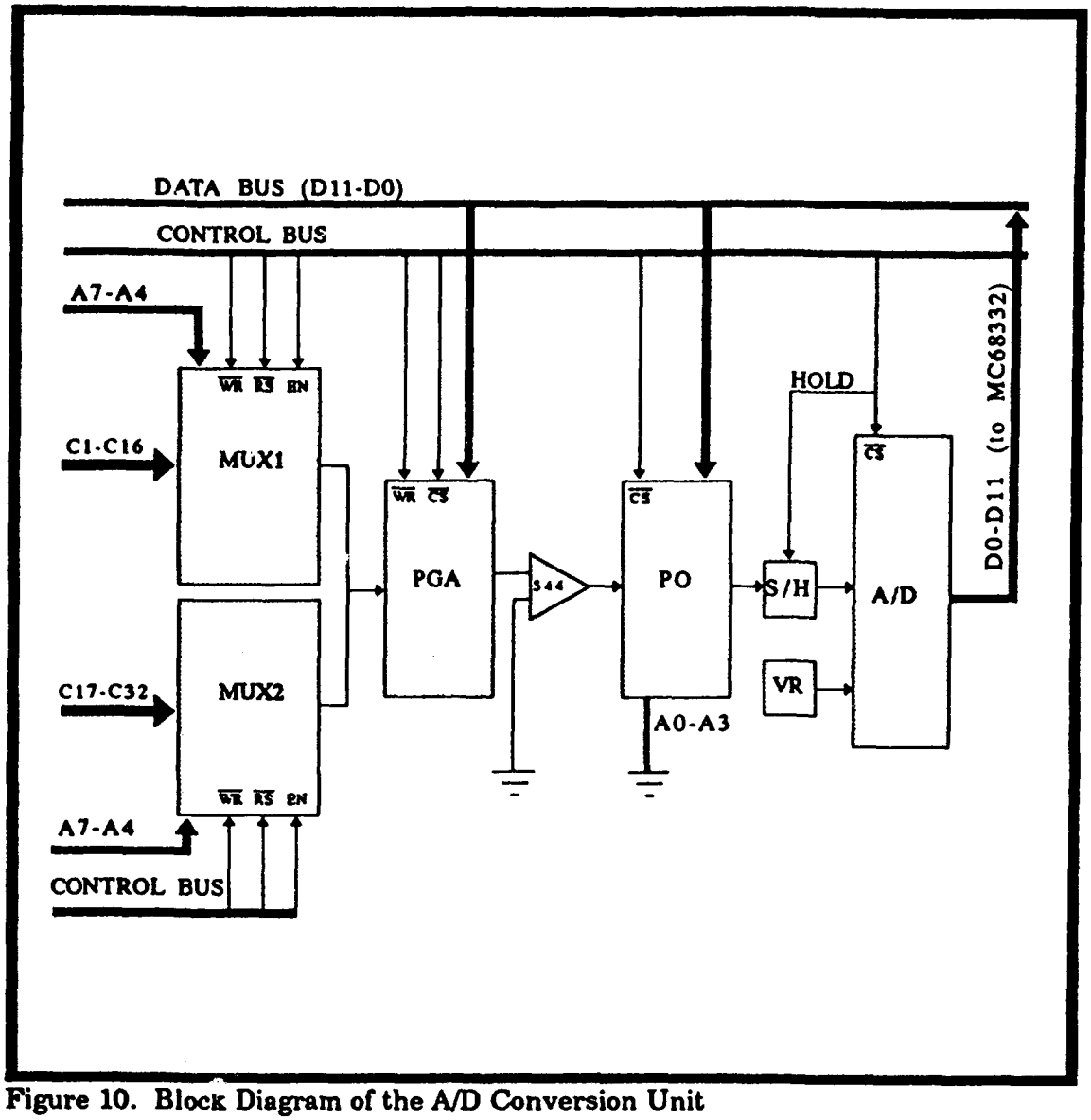


Figure 10. Block Diagram of the A/D Conversion Unit

3.8.1 MULTIPLEXING

Two ADG526A MUXes from Analog Devices Inc., MUX1 and MUX2 in Figure 10, are used to switch from 32 analog input signals to 1. The maximum analog input

signal that these MUXes allow is equal to V_{DD}-2V, which in this case is +13 volts, and the minimum is V_{SS}+2V, which is -13 volts. Therefore, the ±10 volt input range is acceptable because it falls within these limits. The maximum current passing through the signal conditioning devices to the MUXes occurs when the input voltage is 40 volts and is equal to:

$$i = \frac{V}{R} = \frac{V}{R_1 + R_2} = \frac{40}{29.2x10^3+31.6x10^3} = 0.66mA$$

This current is acceptable because it is below the maximum input current of 20mA allowed by the MUX.

Each MUX switches between 16 analog input signals based on a 4-bit digital input code. The analog input signals are connected such that a digital input of i switches channel i+1 to the output. Since address line A0 of the MC68332 is tied low to provide word-only accesses, it cannot be used as part of the digital input code. Therefore, address lines A7-A4 were chosen to switch the MUXes. This input along with the control signals write (WR*), reset (RS*), and enable (EN) are provided by the MC68332.

The outputs of MUX1 and MUX2 are tied together to avoid using an additional MUX. This connection, however, requires that these devices be selected mutually exclusive of each other. For this reason, MUX1 and MUX2 have different chip select ranges to guarantee mutual exclusion. MUX1 will be selected for addresses in the range $83800-$83FFF and MUX2 for $84000-$847FF. Table 4 lists the addresses that must be written to in order to select each channel from the MUXes.

Figure 11 shows the MUX timing requirements for latching the switch

addresses and enable inputs. While WR* is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of WR*. [Analog Devices, 1992] Note that the EN signal must be held a minimum of t_{H1} = 10ns after WR* is negated. This condition cannot be met by simply connecting the MC68332 R/W* signal to the MUX WR* pin and the inverted MC68332

Channel	Address	Channel	Address
Channel 1	$83800	Channel 17	$84000
Channel 2	$83810	Channel 18	$84010
Channel 3	$83820	Channel 19	$84020
Channel 4	$83830	Channel 20	$84030
Channel 5	$83840	Channel 21	$84040
Channel 6	$83850	Channel 22	$84050
Channel 7	$83860	Channel 23	$84060
Channel 8	$83870	Channel 24	$84070
Channel 9	$83880	Channel 25	$84080
Channel 10	$83890	Channel 26	$84090
Channel 11	$838A0	Channel 27	$840A0
Channel 12	$838B0	Channel 28	$840B0
Channel 13	$838C0	Channel 29	$840C0
Channel 14	$838D0	Channel 30	$840D0
Channel 15	$838E0	Channel 31	$840E0
Channel 16	$838F0	Channel 32	$840F0

Table 4. Chip Selection and Switching of Multiplexors

chip select 6 (CS6*) to the MUX EN pin because the CS6* signal is negated before the

R/W* signal is negated. A convenient solution to this problem is to swap the connections. As long as the MC68332 chip select assertion width is greater than the MUX write width and the MC68332 write hold time is greater than the MUX enable width, as illustrated below,

$$t_{S2} > t_{W1} \quad \text{and}$$

$$t_{H2} > t_{H1}$$

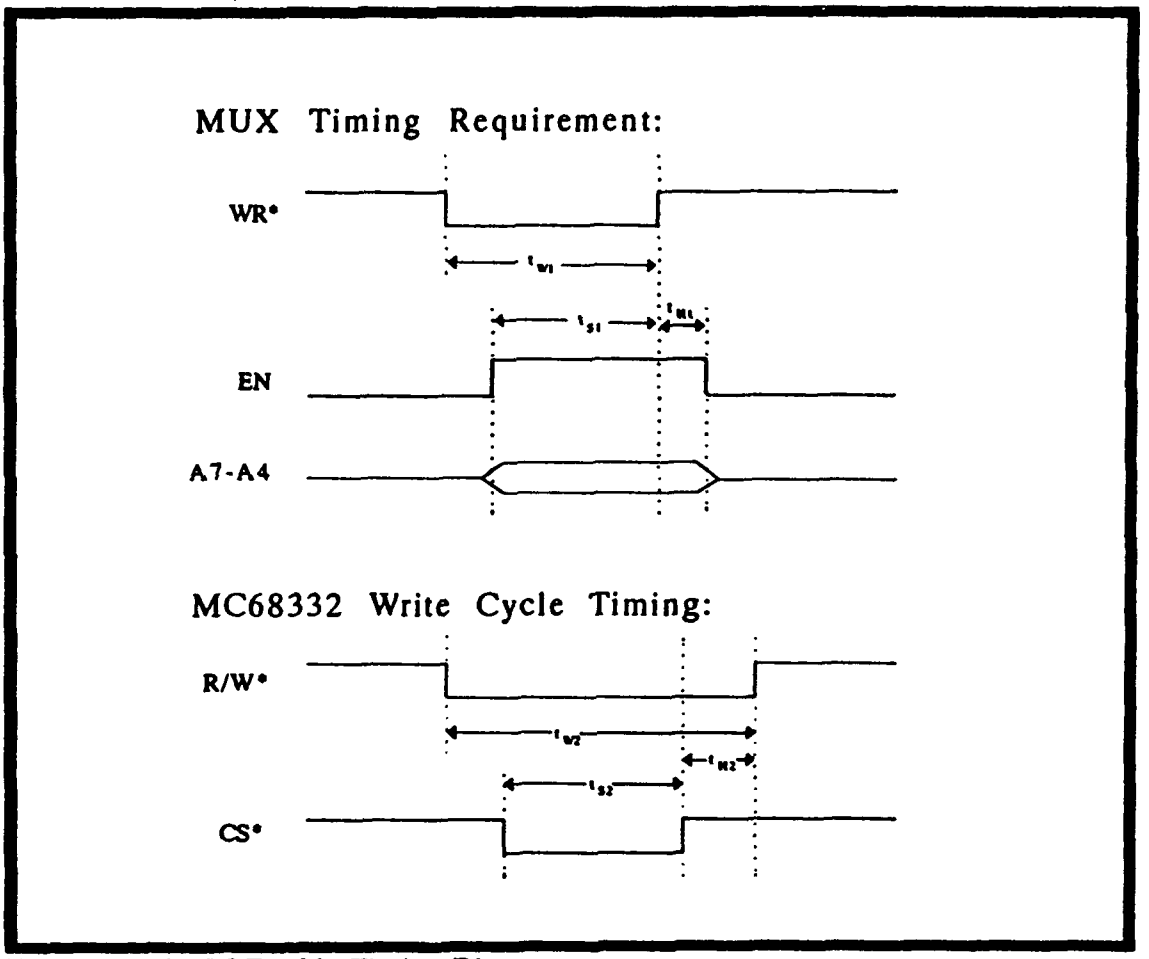


Figure 11. MUX Enable Timing Diagram

the chip select and read/write lines can be swapped, yielding the connections shown in Figure 12. In this configuration, the MUX will be enabled before the WR* signal

is asserted, but this is not a problem since the MUX retains the previous switch condition until the WR* signal is asserted even if the chip is enabled, unless the reset signal (RS*) has been issued. In the case of reset, no channels are switched to the output and the address and enable latches are cleared.

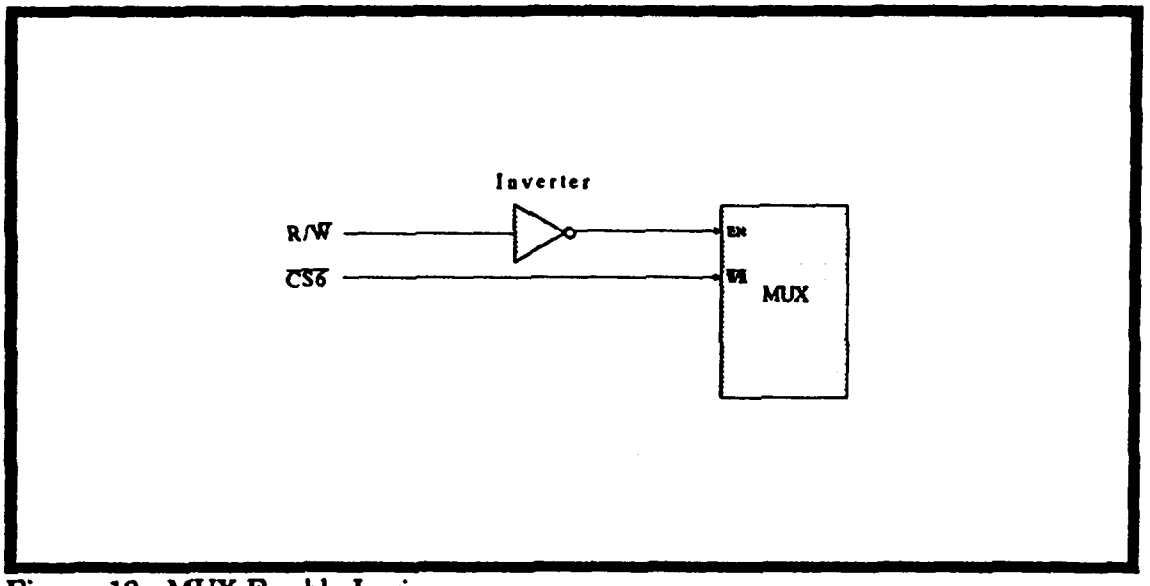


Figure 12. MUX Enable Logic

3.8.2 PROGRAMMABLE GAIN

The Analog Devices, Inc. part number AD7545A is a CMOS 12-Bit buffered multiplying digital-to-analog converter (DAC). This part was used in the second stage of the A/D conversion module to multiply or attenuate the analog input signal by a gain factor. The operational amplifier AD544L is used at the output of the DAC to amplify the signal. Together, these two parts comprise the programmable gain amplification stage, or PGA, as shown in Figure 13. The PGA is configured for

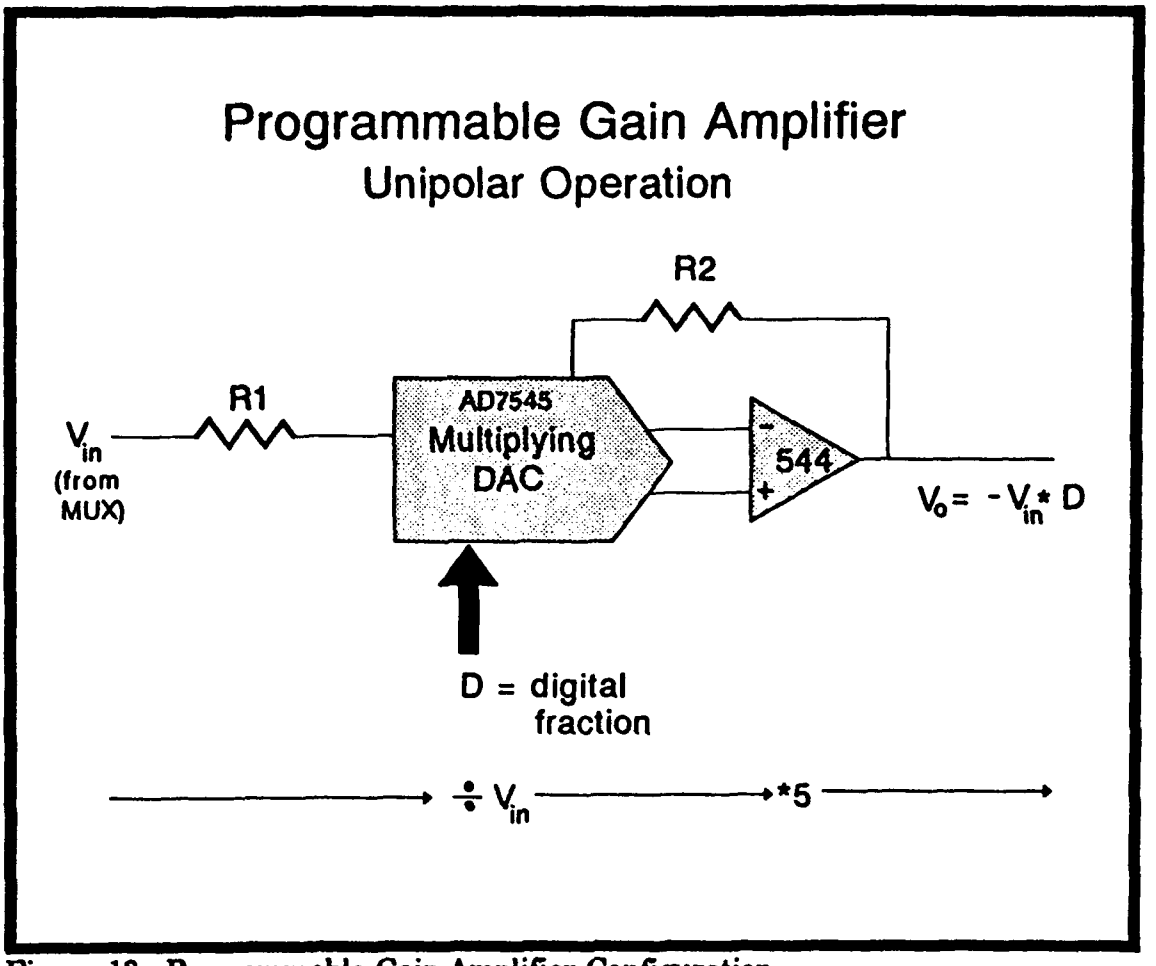


Figure 13. Programmable Gain Amplifier Configuration

unipolar operation as opposed to bipolar, since there is no need to provide a non-inverted output signal. The output of the PGA will be inverted because the DAC output is fed into the inverting input of the 544 OP AMP. An inverted output signal is in fact required by the next stage in order to sum the output of the PGA stage with the output of the programmable offset (PO) stage. The input voltage to the PGA must be between -20 and +20 volts. The equivalent function of the PGA is provided in Table 5. As shown in Table 5, the multiplier is formed by taking the digital binary input and dividing by $2^{12} = 4096$.

The analog output of the PGA stage will be inverted, for both positive and

negative analog input voltages. Notice, however, that the analog input signal to the PGA is multiplied by a fraction and therefore cannot increase in voltage. This is acceptable for channels with large maximum input signals (pre-S/C stage) in the 40 volt range, but when a channel's maximum input signal is smaller than 20 volts, the

12-Bit Digital Input	Analog Output
1111 1111 1111	$-V_{IN} * \frac{4095}{4096} \approx -V_{IN}$
1000 0000 0000	$-V_{IN} * \frac{2048}{4096} = -\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN} * \frac{1}{4096}$
0000 0000 0000	0 Volts

Note: accuracy = ± 2 LSB max. = ± 4.88mV

Table 5. Function of the PGA

resulting signal after the voltage divider circuit in the signal conditioning stage will be less than 5 volts. Since the PGA can only divide this voltage, the maximum input to the A/D converter would be less than the maximum allowed which is 5 volts. If the maximum input signal for a channel is not scaled to the maximum input for the A/D stage, than the full 12-Bit resolution of the A/D converter will not be realized.

To scale each analog input channel, the amplifier connected to the DAC was given additional feedback resistance to provide 5 volt amplification. Thus, the DAC's role is to normalize all of the channels by dividing the input signal by the maximum input voltage for the corresponding channel, and then multiply by 5 to normalize all signals to a 5V max (also shown in Figure 13). Consider a channel that has a 5 volt

maximum input signal. After the divide by 4 network in the signal conditioning stage, the signal reaches the PGA stage at 1.25 volts. The PGA then divides the signal by 1.25 to get a 1 volt signal which is amplified by 5 volts. This configuration is user friendly because the programmer only has to know the maximum voltage for each channel to calculate the digital input to the PGA. The digital inputs to the PGA are stored in a DPRAM table, so that they can be altered in real time if necessary by the main CPU of the flight control computer.

3.8.3 PROGRAMMABLE OFFSET

In the third stage of the A/D Conversion module, the AD667 fixed reference DAC from Analog Devices is used to provide a programmable offset (PO) capability. This stage is necessary to counteract certain constant biases that have been introduced in the analog input signals by external sensors and other devices. The PO DAC works differently than the PGA DAC because its input voltage is fixed, not varied. The 12-bit digital input to the PO determines the voltage level of the output. The PO also has a summing junction input. This input is essentially the negative input of a summing OP AMP; therefore, by connecting the inverted signal from the PGA stage to this summing junction, the outputs of both the PO and PGA are being summed before exiting the DAC, resulting in a noninverted output. Figure 14 illustrates the operation of the PO.

The digital input to the PO is determined as follows:

1LSB = 1/4096 = 2.44mV

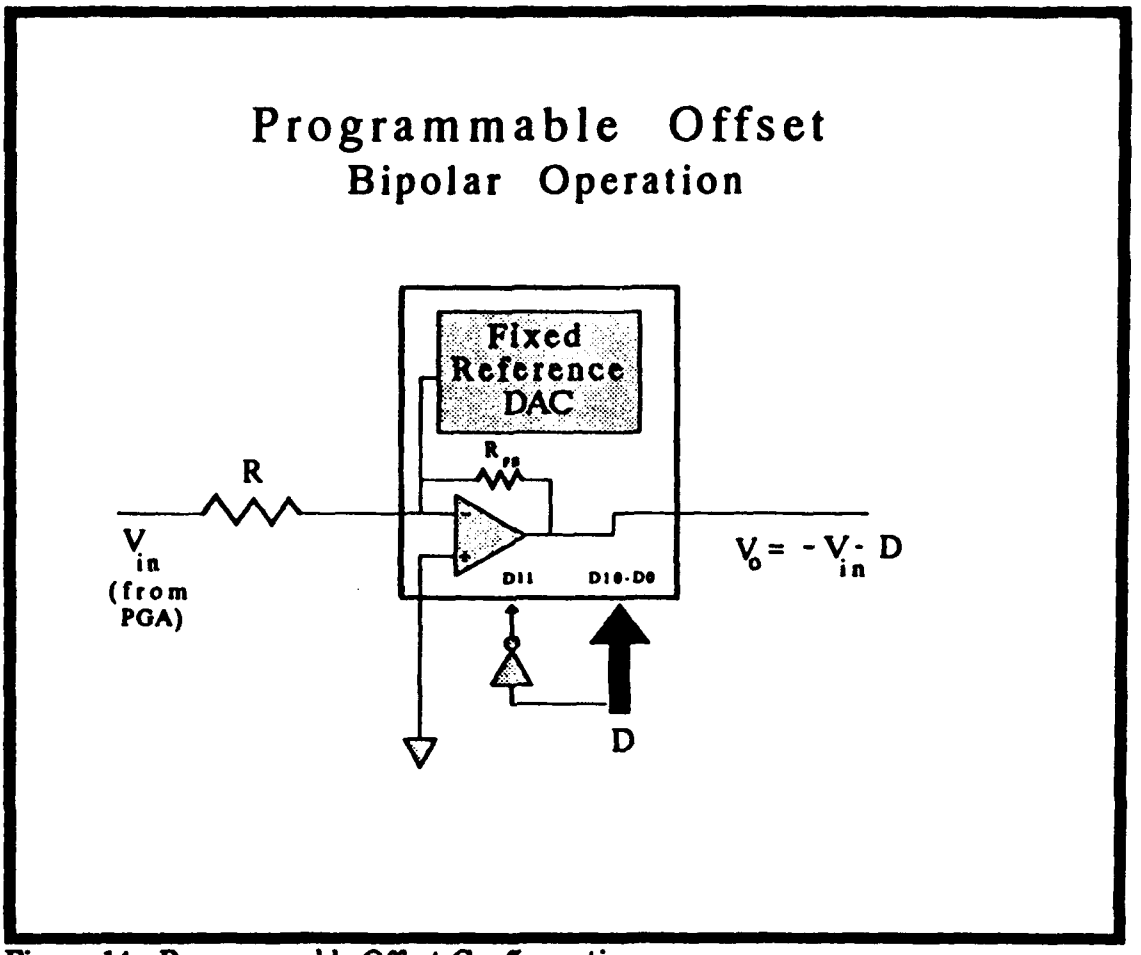


Figure 14. Programmable Offset Configuration

therefore, desired offset = 0.00244 * x

where x = the digital input in decimal.

To compute a negative offset, which is used most often, the two's complement value must be obtained from the hexadecimal equivalent of x. The two's complement implementation is more logical and was included by adding an invertor on the data bit 11 input to the PO. A comparison of the original method and the two's complement is provided in Figure 15.

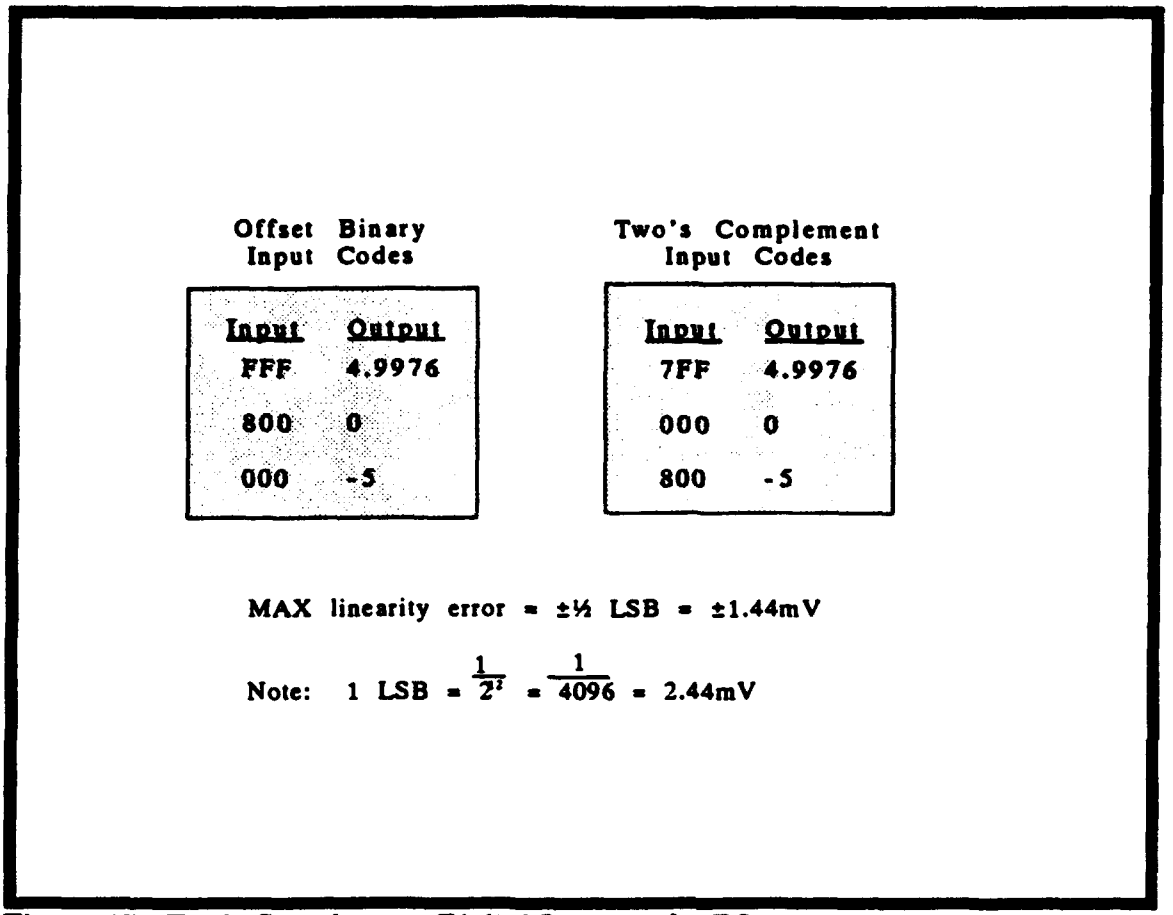


Figure 15. Two's Complement Digital Input to the PO

3.8.4 ANALOG TO DIGITAL CONVERSION

The final stage performs the actual analog to 12-bit digital conversion and is illustrated in Figure 16. The chip select line for the A/D converter is also used to hold the signal at the sample and hold (S/H) device. In order to meet the timing requirement of the S/H device, the chip select for the A/D converter (CS10*) is clocked with the 4 MHz A/D input clock using a J/K flip-flop. Clocking the chip select guarantees that the S/H device has at least two clock periods to hold the input signal

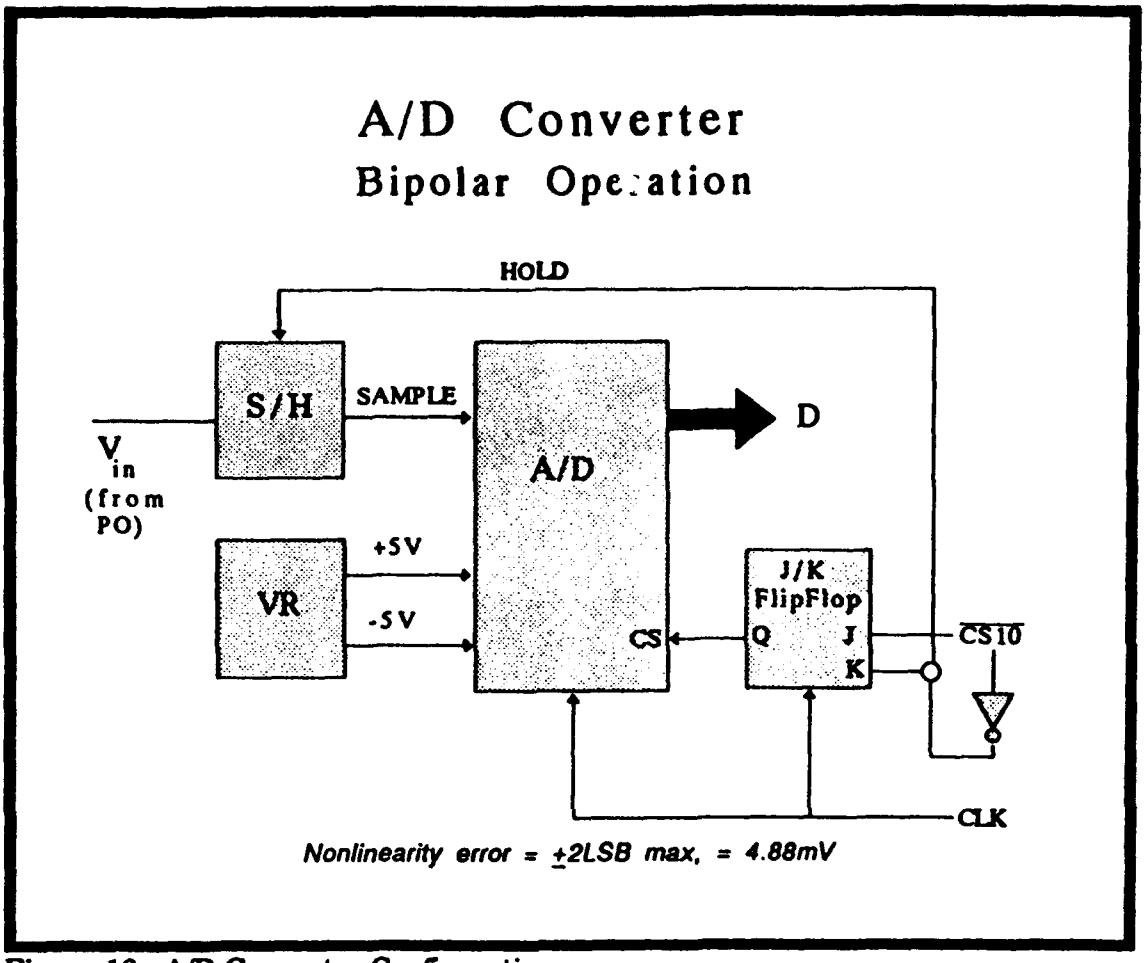


Figure 16. A/D Converter Configuration

and provide an accurate sample to the A/D converter. Since the hold signal is high active, the inverted chip select signal is used. The A/D converter is configured for bipolar operation to allow for +5 to -5 volt input signals. The converter is also configured for fast read mode so that when it is selected, it immediately puts data on the bus from the previous channel and starts conversion of the current channel. The digital result read from the A/D converter by the MC68332 is stored in the dual port RAM so that it can be accessed by an offboard CPU. The analog value can be obtained by multiplying the digital result by 0.00244, which is the voltage equivalent of 1 LSB.

Results taken from the A/D Conversion Unit are shown in Figure 17. The graph in Figure 17 compares the actual results with the desired results and provides a percent error result along the bottom of the chart. The maximum percent error was just below 4 percent. These results include the total errors of the PGA, PO, and A/D

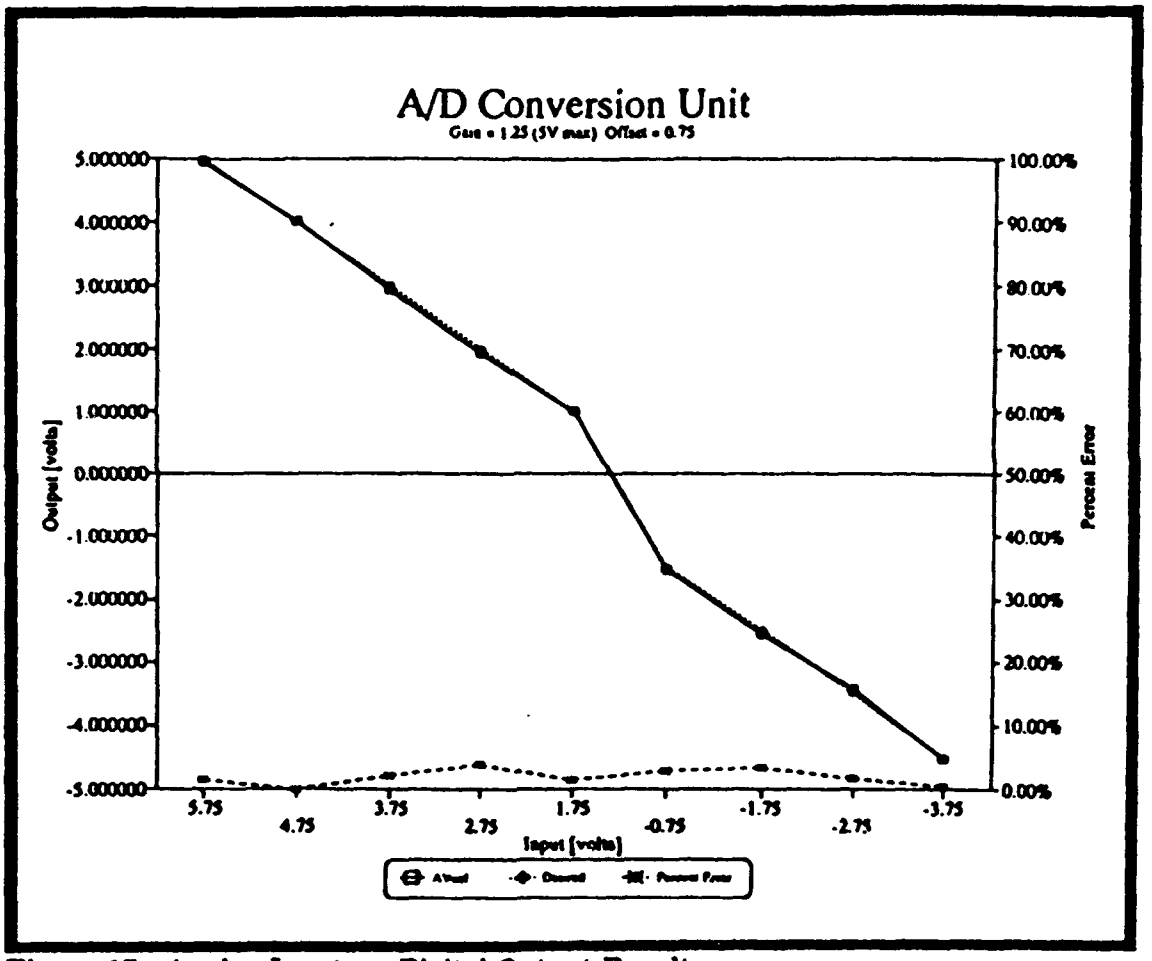


Figure 17. Analog Input vs. Digital Output Results

conversion stage.

3.8.5 A/D CONVERSION MODULE TIMING DELAYS

The timing delays for each stage of the A/D conversion are shown in Figure 18. These delays include the maximum settling time for each device so that the output will be valid after the specified delay. Each stage is processing the current channel, except when the A/D converter is in fast mode, and then the A/D converter is converting the previous channel. The A/D converter does not start converting the current channel until the A/D converter is selected and the new signal is held by the HOLD control line. The digital control of this unit has a different sequence than the other hardware because of the lag by the A/D converter. This sequence is S4, S1, S2, and then S3. This allows the data to be read from the previous channel before a new channel is switched in. The advantage to configuring the A/D converter this way is to avoid having to wait for it to convert the current channel, which would add an additional 5.73μs delay every A/D read cycle. As shown in Figure 18, the A/D conversion module can be updated as fast as 2.68kHz.

3.8.6 PERIODIC INTERRUPT TIMER OPERATION

The MC68332 system integration module (SIM) contains a periodic interrupt timer (PIT), which was used to generate an interrupt periodically to execute the code which controls the A/D Conversion Module. The minimum period allowed by the MC68332 is 122μs. The BCC provides the MC68332 with a crystal so that it can generate a system clock from which the PIT is clocked. Since the BCC does not allow the user to override the crystal circuit, the update frequency of the A/D conversion

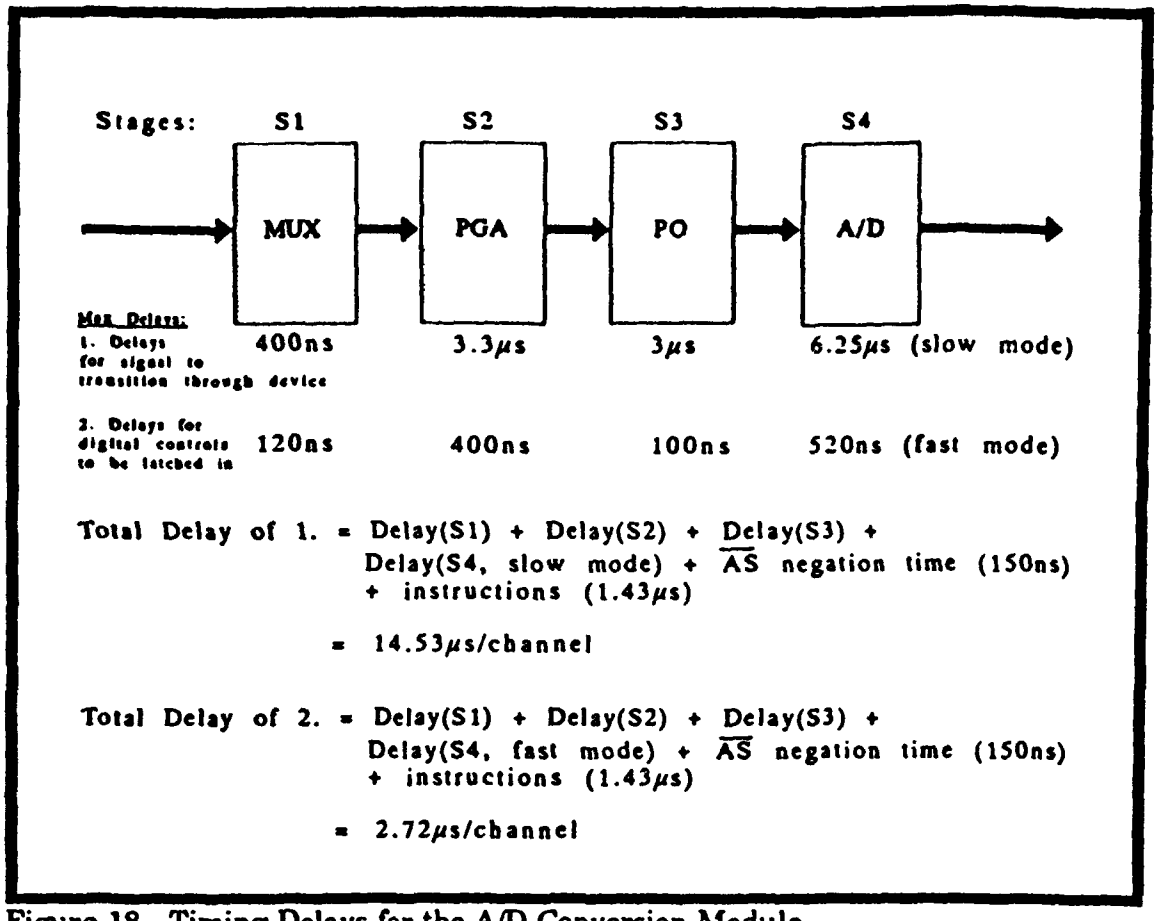


Figure 18. Timing Delays for the A/D Conversion Module

module is limited to 240 Hz. This, however, is only a limit when using the BCC. If the MC68332 were used by itself, a smaller period could be generated by changing the value of the crystal used to generate the system clock in the MC68332. Since the requirement is to update at a better than 50 Hz rate, the configuration with the BCC is acceptable. However, the MC68332 allows much faster interrupt periods, so that future performance improvements can be achieved.

To control the PIT, the periodic interrupt timing register (PITR) and the periodic interrupt control register (PICR) must be initialized. The PITR contains the period at which an interrupt will be generated and the PICR contains the interrupt

handler vector number and the periodic interrupt request level.

By using the PIT, the A/D conversion module control can be interrupt driven, freeing up the MC68332 to control the 16 channels of pulse width modulation. This solution is elegant because the A/D conversion code and the PWM code does not have to be combined or intermixed in any way.

3.9 16 CHANNEL PULSE WIDTH MODULATION

The Time Processor Unit (TPU) on the MC68332 has sixteen orthogonal channels (each channel has the same hardware) which can each be set up to output pulse-width modulated signals. For the I/O controller, the PWM Unit must produce outputs with 2ms periods and a 1-2ms high time. The central processor unit on the MC68332 (CPU32) controls the initialization and updating of the TPU registers. Once the TPU is initialized, it will run independent of the CPU32. Changes can be made at any time simply by updating the TPU registers. The TPU will update its output on the next low-to-high transition of the system clock. The independence of the TPU after initialization frees up the CPU32 to perform other tasks simultaneously.

Table 6 shows the TPU registers which must be updated to perform PWM. The channel function select field must be loaded with $9 to choose the PWM function. This must be done only once during initialization of each channel. The TPU has 9 different functions which it can perform on all 16 channels and each channel can be set to perform different functions. The channel priority field must be set to $1, $2, or $3 for low, middle, or high priority respectively. The channel control parameter, pulse width high time, and the period must be loaded in the proper parameter registers for

each channel. Finally, the host service request (HSR) register must be set to $2 in order to initialize the channel and to start production of the output signal.

After the TPU channels are initialized, the CPU32 executes a loop that fetches updated pulse widths from the dual port RAM and loads them into the TPU pulse width registers to update the pulse widths on each channel. The translation from hex value to the hi-time is determined by a prescaler clock which can be set to divide by 4 or divide by 32. A divide by 32 clock requires a 12-bit value and a divide by 4 clock requires a 16-bit value to produce a 1-2msec hi-time as follows:

[(16.78MHz/32) * 12-bit value = hi-time]

[(16.78MHz/4) * 16-bit value = hi-time]

The 16-bit value was used as shown for various hi-times in Table 6 because it provides more precision than the 12-bit value and thus will generate a better signal.

Channel	Pulse Width 16-bit	Hi-time, msec	Duty Cycle
1	$1060	1.00	50%
2	$1177	1.07	53%
3	$128E	1.13	57%
4	$13A5	1.20	60%
5	$14BC	1.27	63%
6	$15D3	1.33	67%
7	$16EA	1.40	70%
8	$1801	1.47	73%
9	$1918	1.53	77%
10	$1A2F	1.60	80%
11	$1B46	1.67	83%
12	$1C5D	1.73	87%
13	$1D74	1.80	90%
14	$1E8B	1.87	93%
15	$1FA2	1.93	97%
16	$20C1	2.00	100%

Table 6. Pulse Width Modulation Digital Input

3.10 8 DISCRETE OUTPUT CHANNELS

The queued serial module (QSM) of the MC68332 provides serial communication interfaces, but since serial communication is not needed, 8 of its external pins are used as general purpose I/O ports. These ports are initialized to output discrete values, either 0 or 5 volts. The following registers must be configured to set these ports: QMCR, QTEST, QILR, and QIVR. After initialization, these ports can be modified during the operation of the flight control computer by simply updating the registers. This is accomplished through the DPRAM. The MC68332 obtains the updated discrete outputs along with the new PWM values from the DPRAM.

4.0 SOFTWARE

The embedded software was written in MC68332 assembly and encoded on the EPROM. The software was written so that it can be easily relocated to any address range. The only change that must be made to the software if it is moved to a different address range is that the new address of the interrupt handler must be loaded into the interrupt vector table at offset $0100. The 332Bug monitor places the start of the interrupt vector table at $0000, but this can be modified by changing the Vector Base Register (VBR) in the MC68332.

The flowchart for the software is shown in Figure 19. After initialization of the different MC68332 modules, the PIT is initiated so that interrupts will start to occur. The remainder of the program performs a loop that continually updates the PWM channels. The interrupt handler is responsible for controlling the A/D conversion module. Inside the interrupt handler, the first action is to disable the PIT, so that interrupts cannot occur within an interrupt handler. Subsequently, the last action is to reenable the PIT so that interrupts can occur again. This interruption of the interrupt handler adds an additional but minimal delay onto the 240Hz update rate of the A/D conversion module.

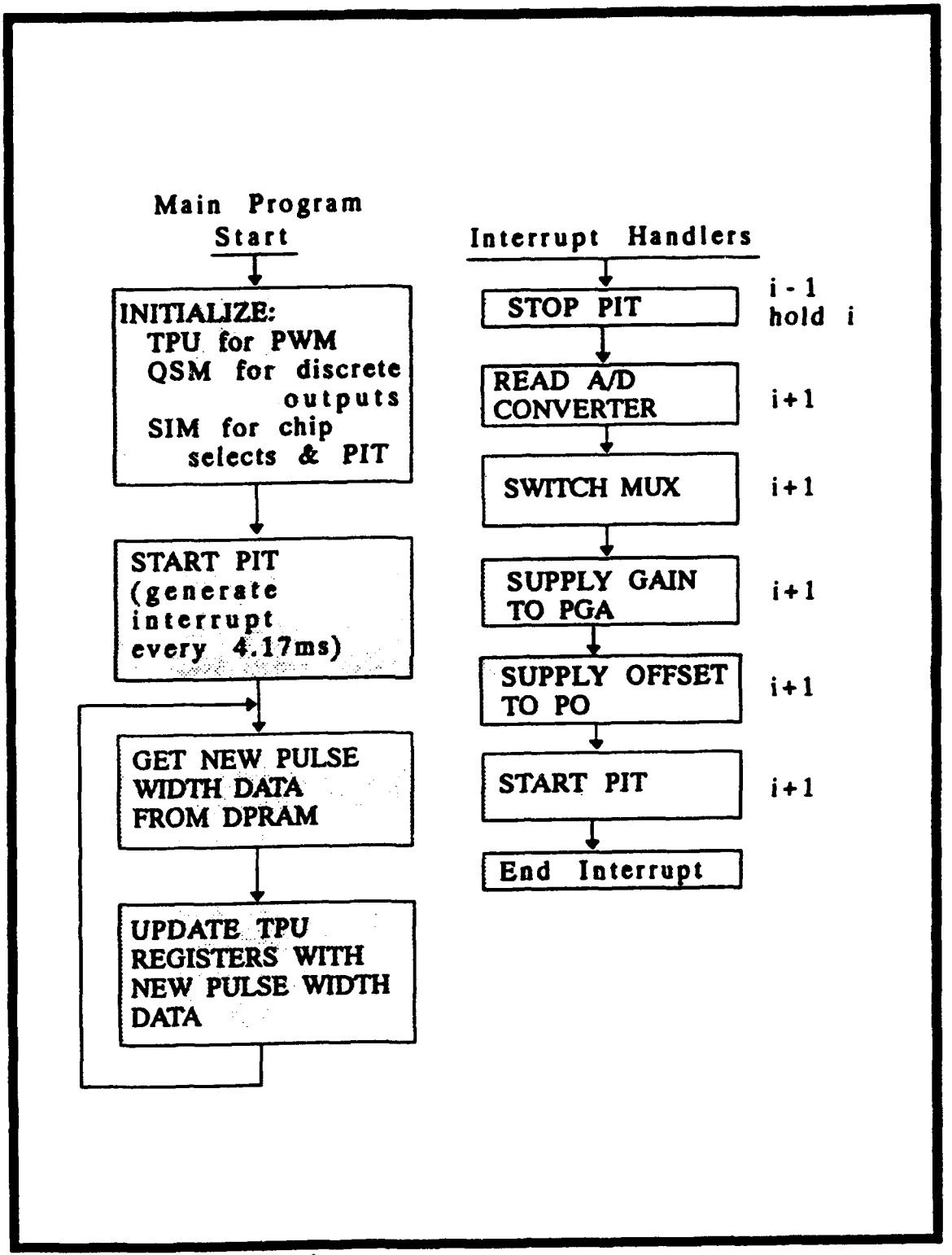


Figure 19. Software Flowchart

5.0 CONCLUSIONS

5.1 DESIGN SUMMARY

The design of the I/O controller system was based on the Motorola MC68332 microcontroller because of the internal modules it contains. These modules, the TPU, SIM, and QSM provide the capability for the MC68332 to control the A/D Conversion, pulse width modulation, and discrete outputs. No other real-time VME-based I/O controller on the market satisfies these requirements. The performance of the I/O controller system developed satisfies the requirements set forth in the problem statement. The A/D conversion module converts 32 channels of analog inputs to 12 bits of accuracy at approximately 240Hz, the PWM module produces 16 channels of pulse width modulated output at a better than 50 Hz, and 8 discrete outputs are generated by the QSM, all on a single 6U VME card.

The digital control and timing of the A/D conversion module was successful. The design exceeded the update requirement that it operate at a better than 50 Hz update rate and it has the potential to operate much faster without the BCC. The digital control allows for complete programmability and minimization. Errors were well within acceptable bounds.

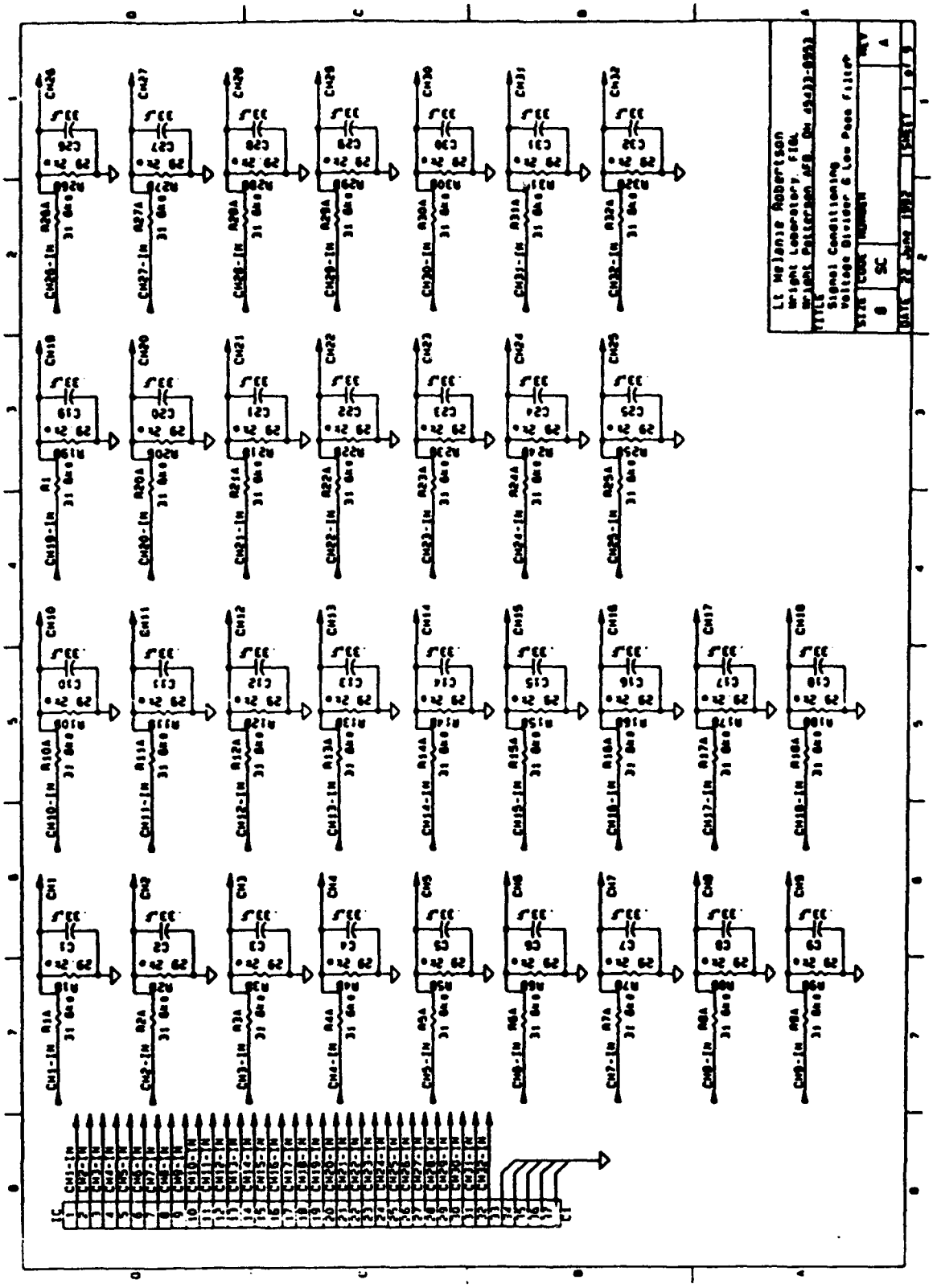
5.2 RECOMMENDATIONS

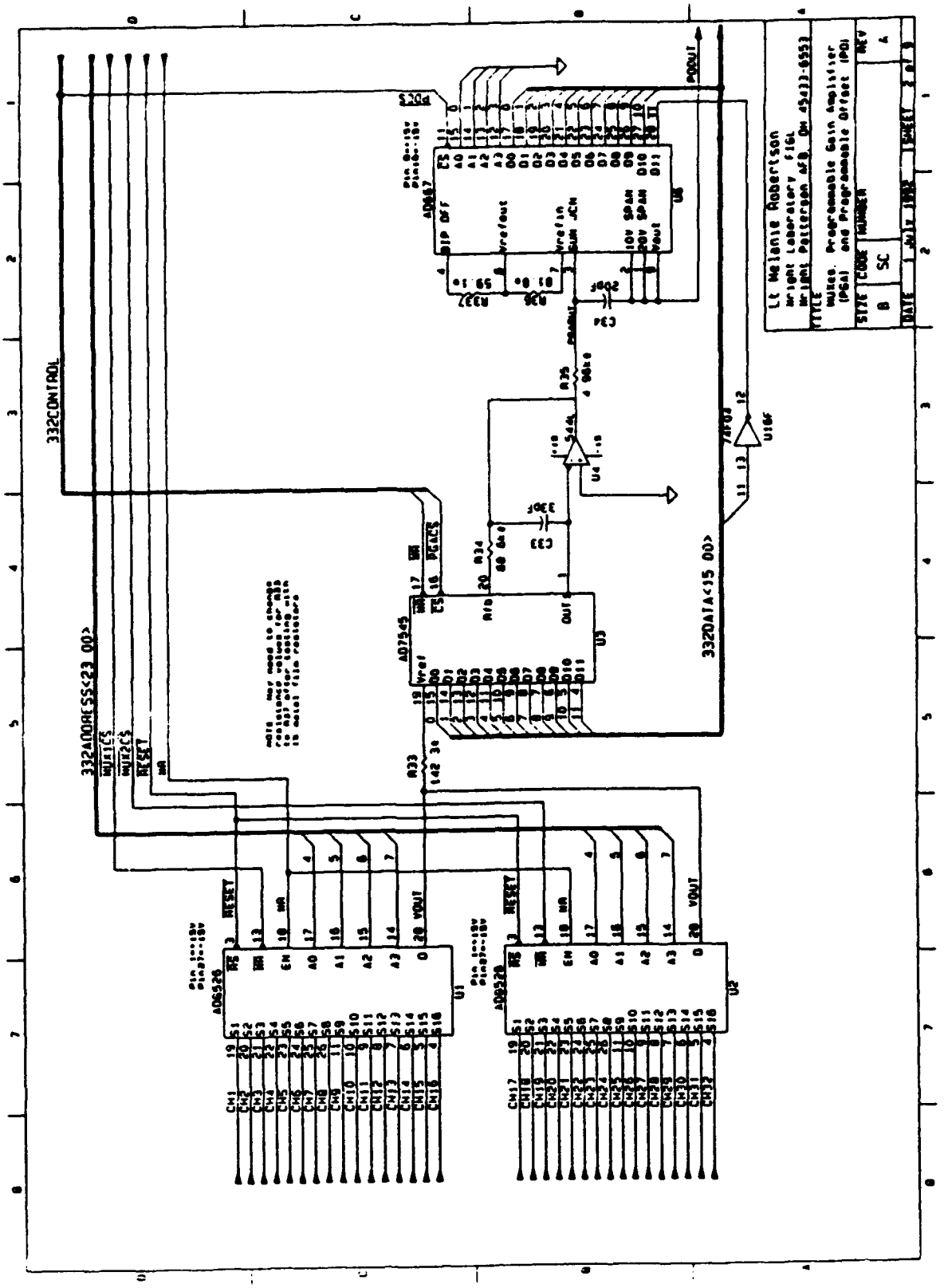
Further minimization and design modifications are recommended to better the system. One change to the requirements that would significantly reduce the size of the I/O controller system is to only allow certain channels to have a 0-±40 volt range. For the remaining channels, the divide by four resistor networks could then be eliminated since most of the analog input signals are currently only 0-±5 volts. This one change could save substantial board space.

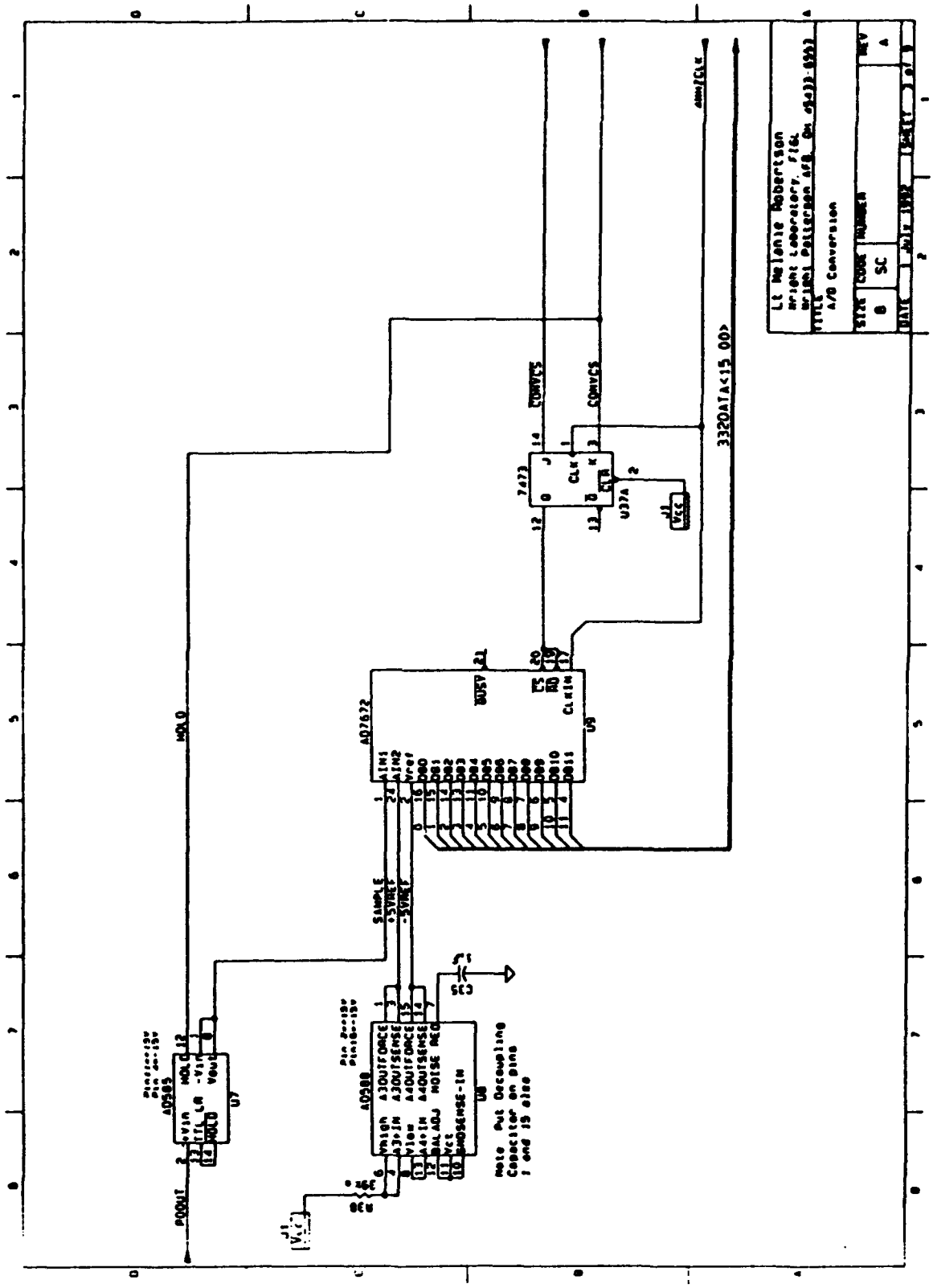
On the design side, there are some changes that could be made to the PGA circuit to provide a gain to every channel. This change would require redesigning the PGA circuit and hardware and the signal conditioning resistors. The result would not change the accuracy of the system, but may make the system a little easier to understand from the user point of view.

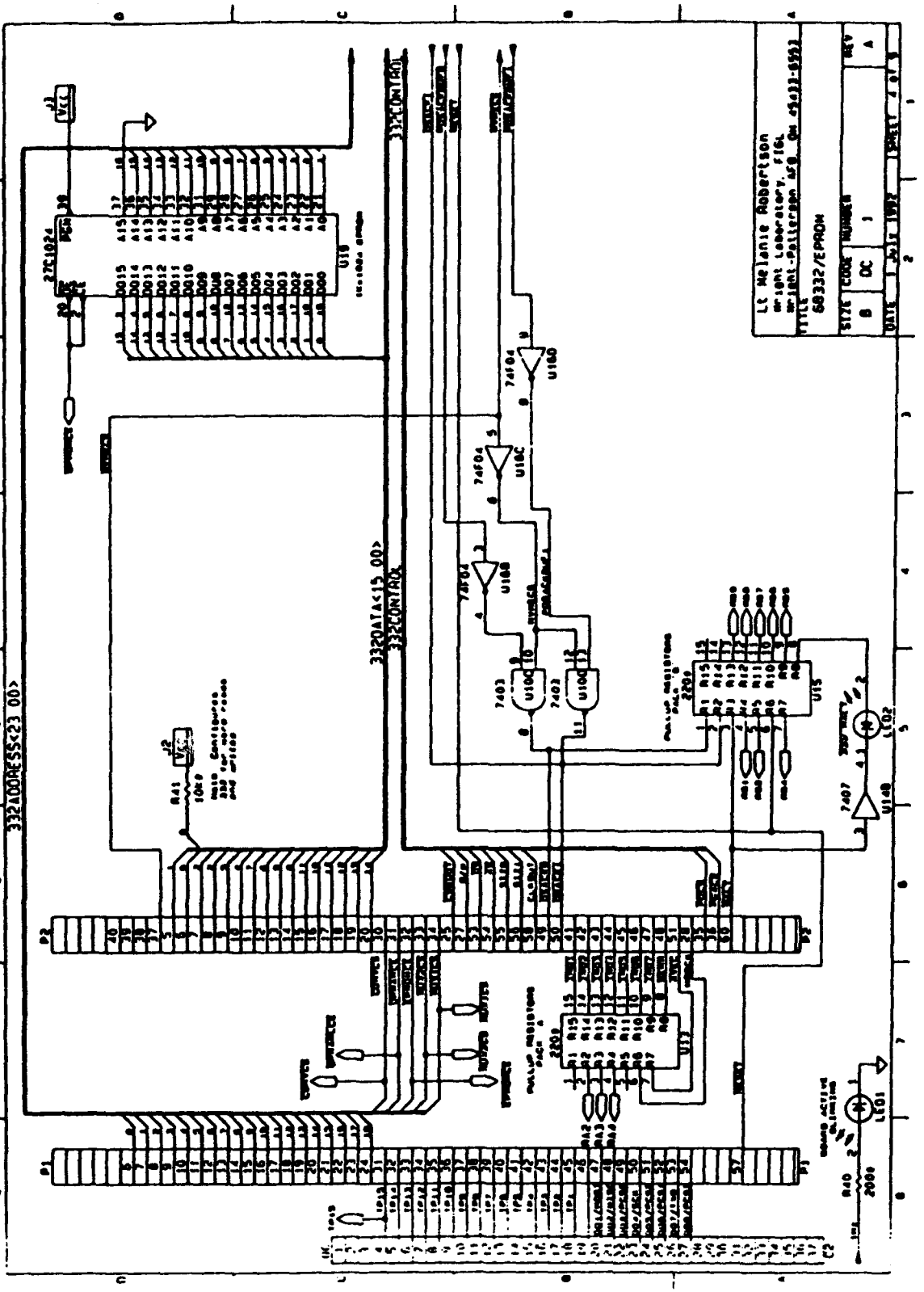
APPENDIX A

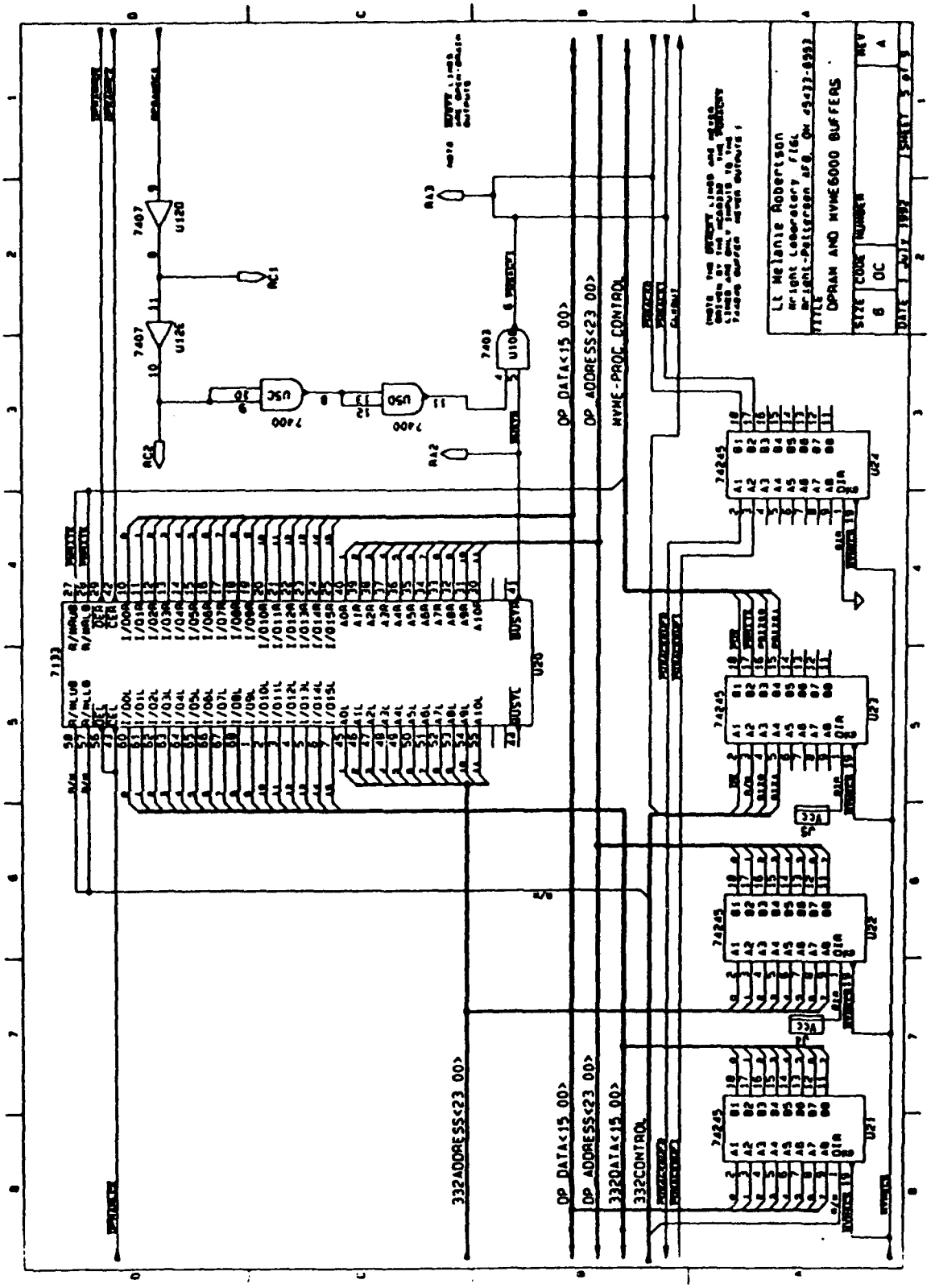
SCHEMATICS

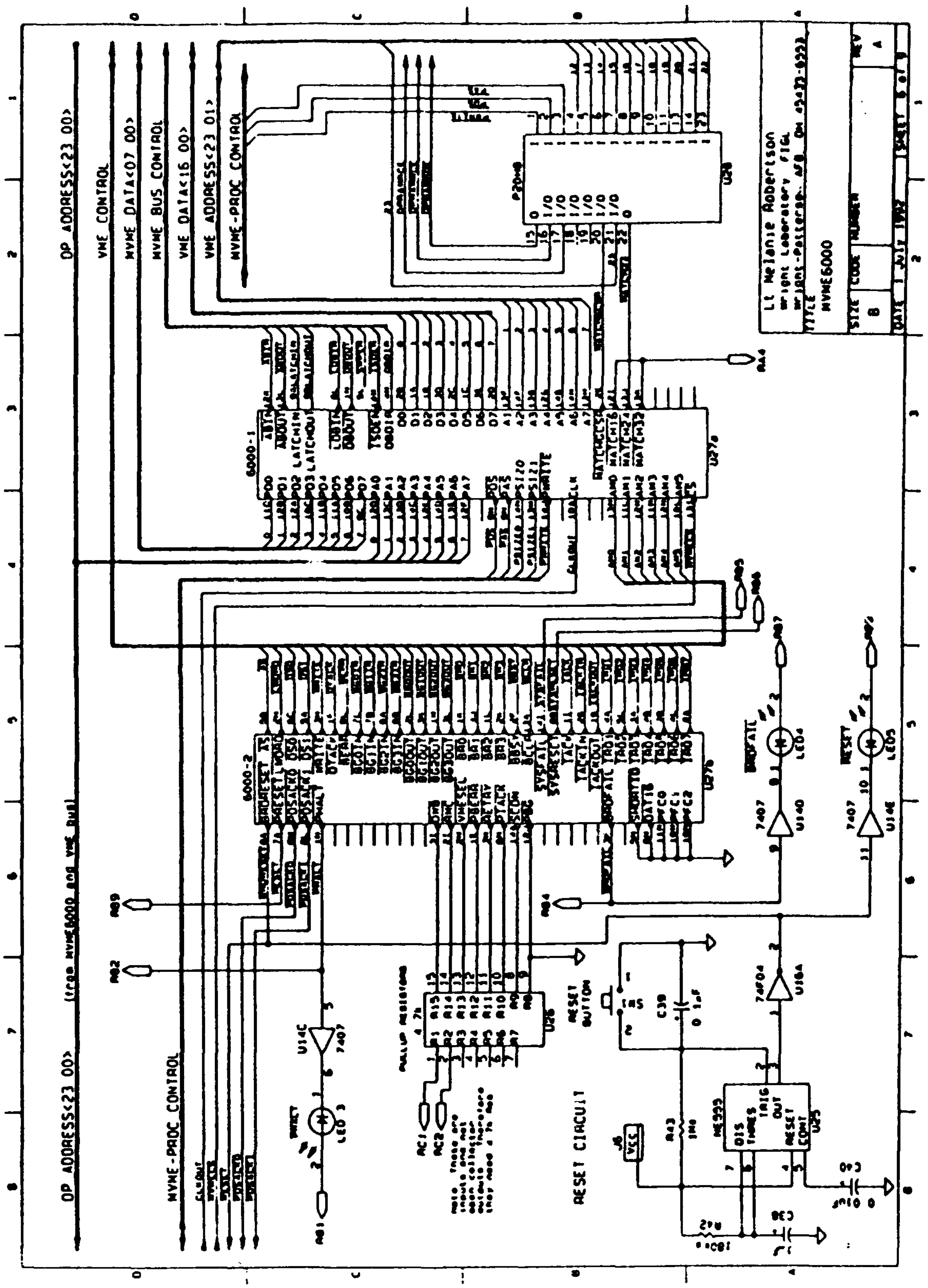


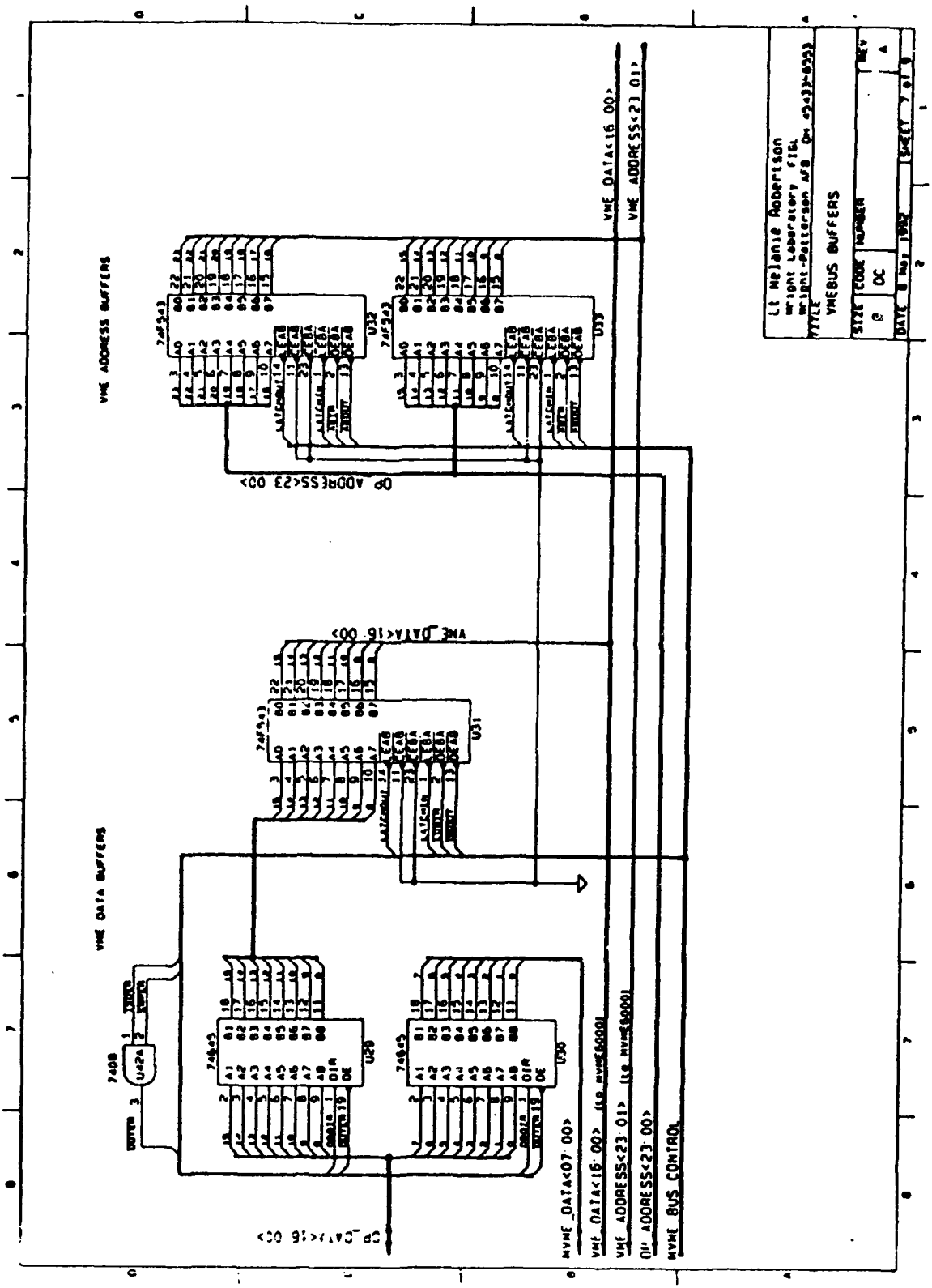

332CONTROL
332ADDRESS<23 00>
332DATA<15 00>
WR1CS
WR2CS
RESET
WR
RDCS
VOUT
RESET
U1
U2
U3
U5
U6
U16
C33
C34
R33
R34
R35
R36
Lt Melanie Robertson
Wright Laboratory, FIGL
Wright Patterson AFB, OH 45433-6553
Multex Programmable Gain Amplifier (PGA) and Programmable Offset (POS)
SIZE
CODE
NUMBER
REV
DATE
SHEET

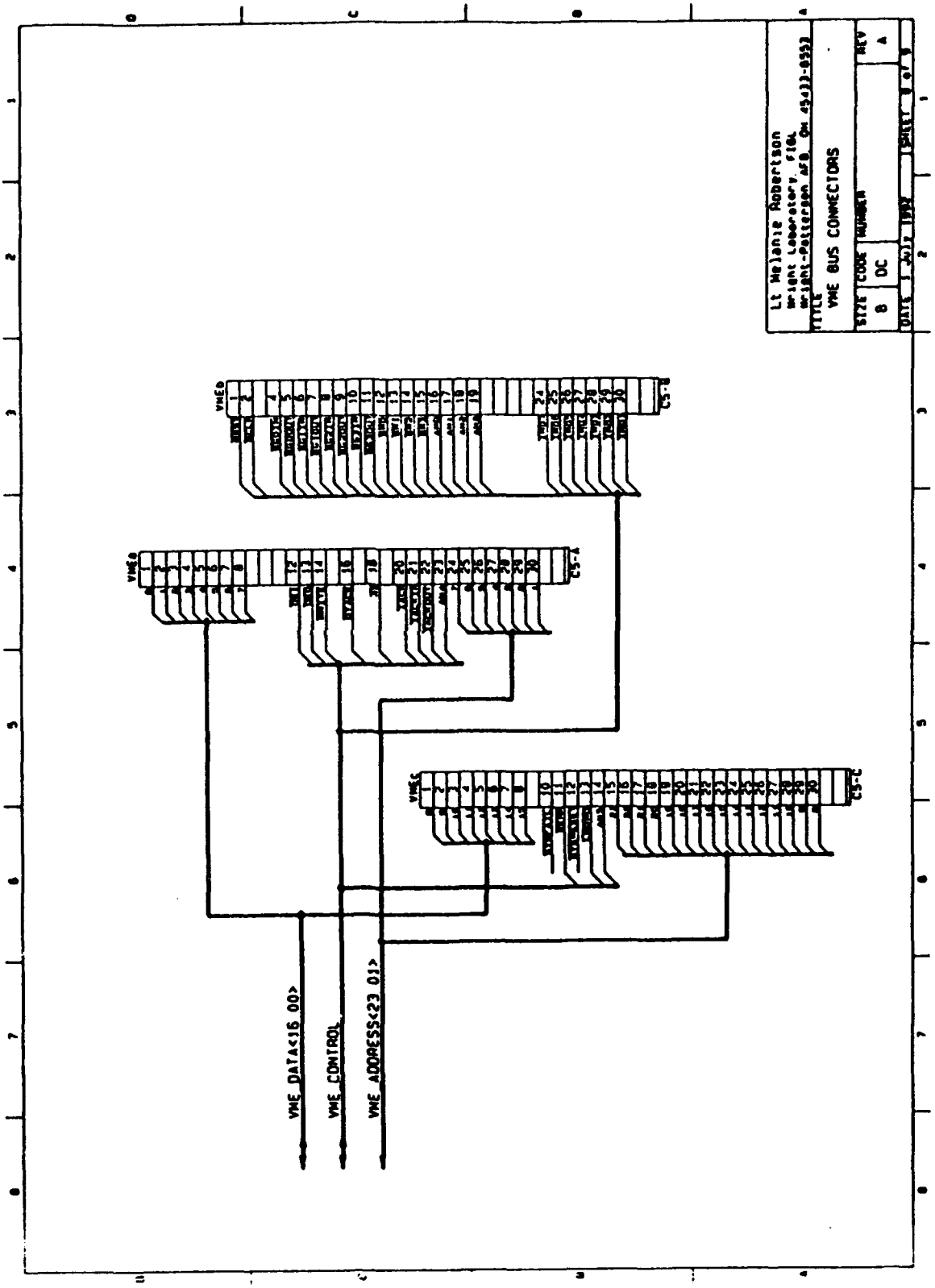

Lt Melanie Robertson
Wright Laboratory, FIGL
Wright Patterson AFB, OH 45433-6543
A/D Conversion
SIZE
B
CODE
SC
NUMBER
REV
4
DATE
Note: Put Decoupling
Capacitor on pins
1 and 15 also
3320DATA<15:00>
CONVCS
AD7672
AD588
AD585
SAMPLE
+5VREF
-5VREF
HOLD
BUSY
CLKIN
VIN1
VIN2
Vref
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
A3OUTFORCE
A3OUTSENSE
A4OUTFORCE
A4OUTSENSE
NOISE RED
BIPOLAR-IN
VPOS
VNEG
A3+IN
A3-IN
A4+IN
A4-IN
BIPOLAR ADJ
U7
U8
U9
U37A
7473
+5V

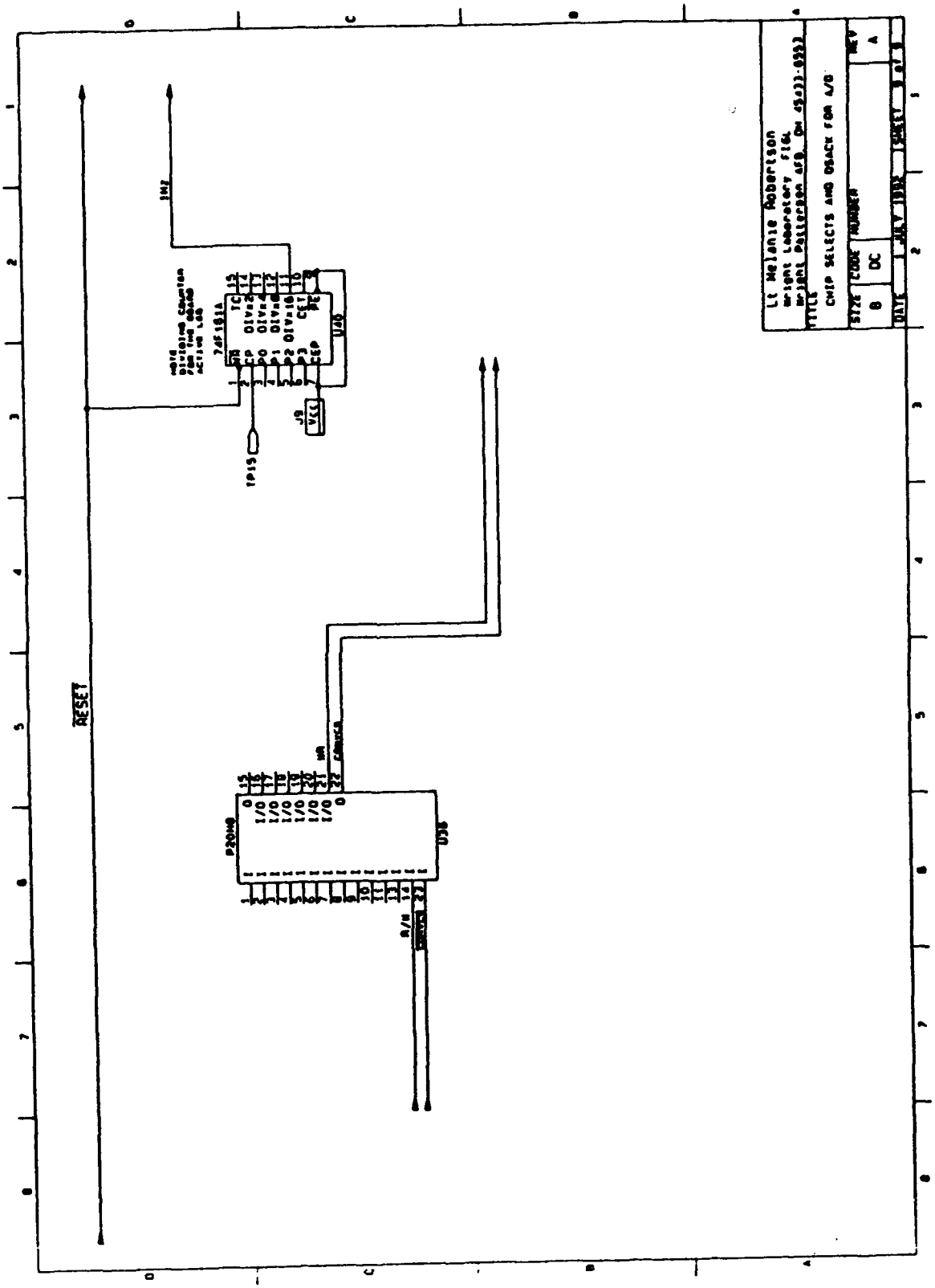



OP DATA<15 00>
OP ADDRESS<23 00>
NVME-PROC CONTROL
332ADDRESS<23 00>
332DATA<15 00>
332CONTROL
Lt Melanie Robertson
Wright Laboratory /FIGL
Wright-Patterson AFB, OH 45433-6533
OPRAM AND NVME6000 BUFFERS
SIZE B
CODE 0C
REV A
DATE 2/17/1992
SHEET 5 OF 5


OP ADDRESS<23 00>
VME CONTROL
MVME DATA<07 00>
MVME BUS CONTROL
VME DATA<15 00>
VME ADDRESS<23 01>
MVME-PROC CONTROL
6000-1
6000-2
PULLUP RESISTORS
RESET BUTTON
RESET CIRCUIT
Lt Melanie Robertson
Wright Laboratory FIGL
MVME6000
SIZE
CODE
NUMBER
REV
DATE
SHEET


VME ADDRESS BUFFERS
VME DATA BUFFERS
VME DATA<16 00>
VME ADDRESS<23 01>
OP ADDRESS<23 00>
OP_DATA<16 00>
MVME BUS CONTROL
VMEBUS BUFFERS
Lt Melanie Robertson
Wright Laboratory, FIGL
Wright-Patterson AFB OH 45433-6553
SIZE
CODE
NUMBER
REV
DC
SHEET 7 of 9


Lt Melanie Robertson
Wright Laboratory, FIGL
Wright-Patterson AFB, OH 45433-6553
VME BUS CONNECTORS
SIZE
B
CODE
DC
REV
A
VME0
VME1
VME2
P1-J2
P1-J1
P2-J2
VME_DATA<15 00>
VME_CONTROL
VME_ADDRESS<23 01>


RESET
INT
U26
U36
TP15
Lt Melanie Robertson
Wright Laboratory FIGL
Wright Patterson AFB, OH 45433-6553
CHIP SELECTS AND DBACK FOR I/O
SIZE
CODE
NUMBER
REV
DATE
SHEET

APPENDIX B

PARTS LIST

PART NUMBER(s)	DEVICE	DESCRIPTION
U1, U2	ADG526AKN	CMOS Latched 8/16 Channel Analog Multiplexer
U3	AD7545JN	CMOS 12-Bit Buffered Multiplying DAC
U4	AD544KH	High Performance, BiFET Operational Amplifer
U5, U16	SN74F04	Fast TTL Hex Inverter
U6	AD667JN	Microprocessor-Compatible 12-Bit D/A Converter
U7	AD585AQ	High Speed, Precision Sample-and-Hold Amplifier
U8	AD588AD	High Precision Voltage Reference
U9	AD7672KN03	LC^{2}MOS High-Speed 12-Bit ADC
U10	SN7403	TTL Quad 2-Input NAND Gate (with Open Collector High-Voltage Output)
U11	SN7432	TTL Quad 2-Input OR Gate
U12, U14	SN7407	TTL Hex Buffer/Driver (with Open Collector High-Voltage Output)
U13, U15	resistor pack	15 220Ω resistors
U17	clock	32 MHz
U18, U28, U36, U39	GAL20H8A	Generic Array Logic Device
U19	AM27C1024-150DC	1 Megabit (65,536 x 16-Bit) CMOS EPROM

PART NUMBER(s)	DEVICE	DESCRIPTION
U20	IDT7133S55G	32K (2K x 16-Bit) CMOS Dual-Port RAM
U21, U22, U23, U24	SN74F245N	Fast Octal Bus Transceiver (with 3-State Outputs)
U25	NE555	Single Timing Circuit
U26	resistor pack	15 4.7kΩ resistors
U27	MVME6000AC	VMEbus Interface
U29, U30	SN74ALS645A-1	Octal Bus Transceivers (with 3-State Outputs)
U31, U32, U33	SN74F543	Fast Octal Registered Transceiver, Non-Inverting (with 3-State Outputs)
U34	clock	20 MHz
U35, U38, U40	SN74F161A	Fast Counter
U37	clock	2.4576 MHz
C1, C2	BCC	Business Card Computer Connectors
R1A-R32A	31.6kΩ resistor	1% metal thin film, ¼ Watt
R2B-R32B	10.5kΩ resistor	1% metal thin film, ¼ Watt
R33	143Ω resistor	1% metal thin film, ¼ Watt
R34	68.1kΩ resistor	1% metal thin film, ¼ Watt
R35	4.99kΩ resistor	1% metal thin film, ¼ Watt
R36	82.5Ω resistor	1% metal thin film, ¼ Watt
R37	59.0Ω resistor	1% metal thin film, ¼ Watt
R38	39.2kΩ resistor	1% metal thin film, ¼ Watt
R39	1kΩ resistor	1% metal thin film, ¼ Watt
R40	200Ω resistor	5% fixed composition, ¼ Watt
R41	10kΩ resistor	5% fixed composition, ¼ Watt
R42	180kΩ resistor	5% fixed composition, ¼ Watt
R43	1MΩ resistor	5% fixed composition, ¼ Watt

PART NUMBER(s)	DEVICE	DESCRIPTION
C1-C32	0.33μf capacitor	ceramic
C33	33pf capacitor	ceramic disc
C34	20pf capacitor	ceramic disc
C35	1μf capacitor	tantalum
C36	470pf capacitor	capacitor disc
C38	1μf capacitor	tantalum
C39	0.1μf capacitor	tantalum
C40	0.01μf capacitor	ceramic disc
LED 1-5	red LED	
SW1	reset switch	

APPENDIX C

PRODUCT LITERATURE BIBLIOGRAPHY

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APPENDIX D

PRINTED CIRCUIT BOARD LAYOUT

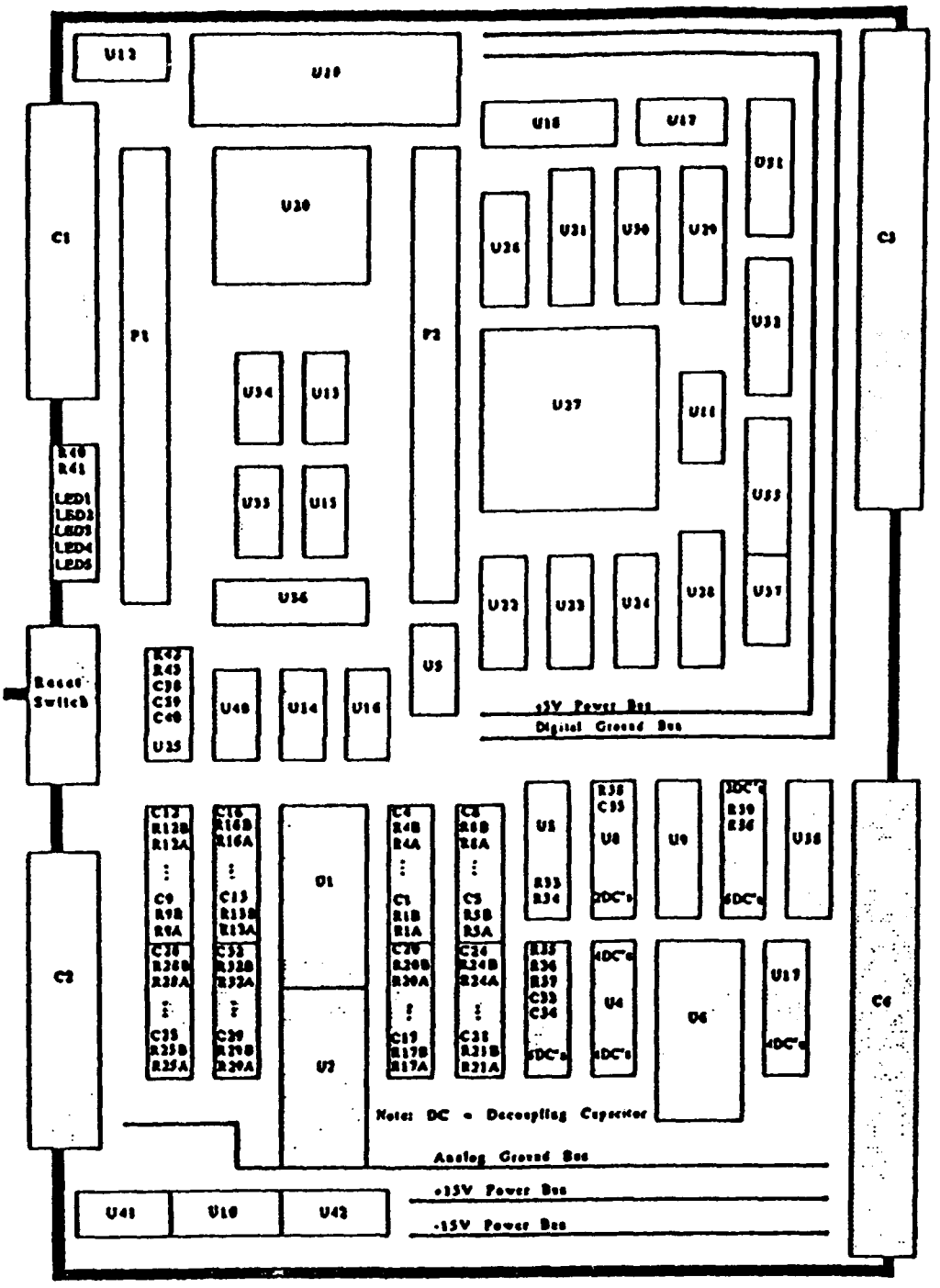

Figure 20. Printed Circuit Board Layout

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VITA

Melanie M. Robertson was born on 23 June, 1966 in Reading, Pennsylvania. She graduated with honors from Hamburg Area High School in Hamburg, Pennsylvania in 1984 and then attended The George Washington University in Washington DC, where she received a Bachelor of Science Degree in Electrical Engineering with a Computer Engineering option in 1988. During her studies at The George Washington University, she concentrated on the design and testing of a VLSI CMOS multiplier chip. Other projects included development of a menu-driven software program to provide subway routes at an information kiosk and the design of a graphical user interface for stationary bicycles. Also during her four year undergraduate program, she was a cadet in the United States Air Force Reserve Officer Training Corps (ROTC) at Howard University, Washington DC. In 1988, she completed the ROTC program as a Distinguished Military Graduate and received a regular commission in the United States Air Force. After graduation and commissioning, she was stationed at the Foreign Technology Division at Wright Patterson Air Force Base, Ohio. In September 1989, she began the Master's program in Computer Engineering at Wright State University in Dayton, Ohio.